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Investigating the feasibility of using nanobridge weak links as the active Josephson element in Rapid Single Flux quantum circuitry

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I, Abubakar Adan, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Abstract

Josephson junctions are used in present day voltage standards. To extend their use to AC voltage standards a high bandwidth, low-noise detector is required. A candidate component for this detector is a superconducting comparator based on Rapid Single Flux Quantum (RSFQ) circuits. The work presented here is a study to determine if nanobridge weak links can be used as the active Josephson element in these circuits. In order to achieve this an understanding of the nanobridge properties and in particular their critical currents is fundamental. We present simulations of a simple comparator using the circuit simulation software JSIM in order to study the effect of varying nanobridge parameters such as width, length, and loop area. These geometrical variables have an affect on the critical currents and loop inductances which subsequently effect device performance. Particular emphasis is given to investigation of how these parameters affect a key figure of merit, the grey zone width.

Acknowledgements

I would like to express my gratitude to both of my supervisors, Dr Edward Romans and Dr Jonathan Williams for introducing a chemist to the wonderful and frustrating world of Josephson junctions. It has been an amazing experience and I thank them wholeheartedly, not only for their tremendous academic support, but also for giving me so many wonderful opportunities to expand my knowledge. I want to thank Dr Connor Shelley for his valuable advice and help throughout this project, and to my colleague Arnaud Blois whose help at the beginning of this project was invaluable. I would like to express my gratitude to all the cleanroom staff: Steve Etienne, Mike Cresswell and Suguo Huo for their constant efforts into maintaining the equipment and for sharing their expertise in the different processes. I would also like to thank (soon to be Drs) Thuong Thuong Nguyen, Nick Constantino and Nuno Braz, for keeping me sane throughout this writing process. I also would like to issue a special mention to Samuel Esilaba, Bubz Haque and Renee Barrett (as our saying goes "Started From The Bottom Now We're Here!").

On a personal level, I would like to thank all my family and dedicate this Thesis to them for their continuous encouragements, love and attention. In particular, I thank my parents Khadra Nur and Mohammed Ali for the support and encouragement through the past couple of years and especially at the end. Finally, I would like to thank my beautiful, loving, supportive and encouraging partner Tahmina Karimova, for everything she has done to help me during this project.

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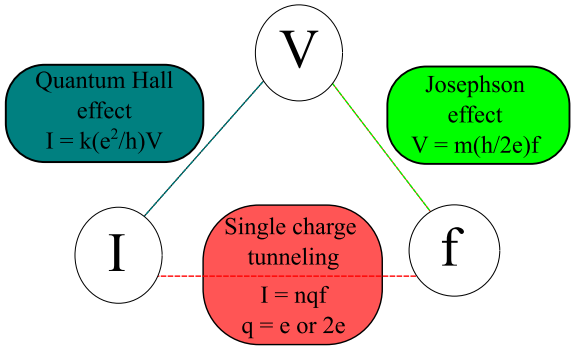


Figure 1: The quantum metrological triangle, reflects the fundamental relationships between the basic electrical quantities, namely the voltage, current and frequency, given by quantum mechanical laws. The numbers k, m and n are integers.

Research into the field of electrical metrology focusses on the development of quantum standards. The main goal is the realisation of electrical quantities in terms of the fundamental constants, electron charge e and Plank's constant h. A voltage standard based on the Josephson effect was the first true step towards quantum electrical metrology [1–4]. This was followed a decade later by the quantised Hall effect, based on the von Klitzing constant [5, 6] which allows the ohm to be maintained very precisely. A quantum current standard is yet to be fully realised. Nevertheless, recent developments suggest that there are many different possible manifestations in which a quantum current standard could be realised [7–10]. Taken together these three quantum standards, define the quantum electrical triangle of standards shown in Figure 1. The units can be realised in terms of different combinations of e and h. Although the DC voltage standard is well established

there is still plenty of demand for research on AC voltage standards.

Early research focused on development of two types of methods for achieving an AC voltage standard: i) the Josephson Arbitrary Waveform synthesiser (JAWS) [11–14] which exploits the Josephson relation of flux quantisation to generate a voltage output from high frequency pulse, and ii) the Programmable Josephson Voltage Standard (PJVS) [15–17] using an array of Josephson junctions biased in such a way to create a staircase AC wave. Both methods suffer from significant drawbacks (see section 1.4) and have been restricted to low frequency AC waveforms. More recent work has focused on utilising very fast Rapid Single Flux Quantum circuitry (RSFQ) in the form of Analogue to Digital converters as a means towards a high frequency AC voltage standard, through the use of a Josephson comparator as the main signal processing and decision making element of the circuit. The measure of the performance of a Josephson comparator is its grey zone, which describes the decision uncertainty of the comparator, represented as a finite transition of width between logical states "0" and "1" and arises as a result of smoothing due to thermal noise. Previous work has lead to much understanding of this limiting factor from both a theoretical and an experimental point of view. In Chapter 2 we review recent progress in the development and testing of Josephson comparators.

The main existing method of fabricating the active Josephson element in RSFQ circuits utilises complex multilayer tunnel junction technology with low T_c material [18–21] or through the use of grain boundary junctions in high T_c [22] materials. Although the processes are well established they do require several steps to yield active devices, and their complexity reduces the ability to integrate these circuits into other devices such as optical or microwave circuits. This report investigates the feasibility of using nano-bridge weak links as the active Josephson element of Josephson comparators in an RSFQ logic circuit. The ease of fabrication and the ability to integrate and fabricate other components on a single chip makes it a very attractive means of obtaining complex integrated circuitry in a few steps. In Chapter 3 we discuss the lithographic approaches used by various groups to

pattern and fabricate nano-bridge weak links. We use this to discuss initial design parameters for the low T_c Josephson comparator and introduce the circuit and inductance simulation tools, JSIM and 3D-MLSI.

Using both JSIM and 3D-MLSI we perform and report on simulations that describe operational performance of a low T_c nanobridge comparator based on a design first introduced by Oelze *et al.* [23] for high T_c films. We discuss the effect of biasing, inductance distribution and temperature variation on device performance, and determine optimal operational parameters and biasing margins. In Chapter 5 we discuss the issues that arise from variations in the electrical parameters of in fabrication yields of nano-bridge weak links such critical current spreads due to fluctuations in the fabricated of weak link. We also discuss the viability of perorming measurements close to T_c to minimise heating effects in the nanobridge. We discuss effect of high critical currents at temperatures much lower than T_c and the resulting effect on the grey zone. Finally we draw conclusions for the conditions that result in optimal comparator operation resulting in the smallest grey zone.

Chapter 1

Theoretical Background

1.1 Superconductivity

Superconductivity is a phenomenon of exactly zero electrical resistance and expulsion of magnetic fields occurring in certain materials when cooled below a characteristic critical temperature T_c. It was discovered by Dutch physicist Heike Kamerlingh Onnes on April 8, 1911 in Leiden when studying the resistance of solid mercury at cryogenic temperatures [24].

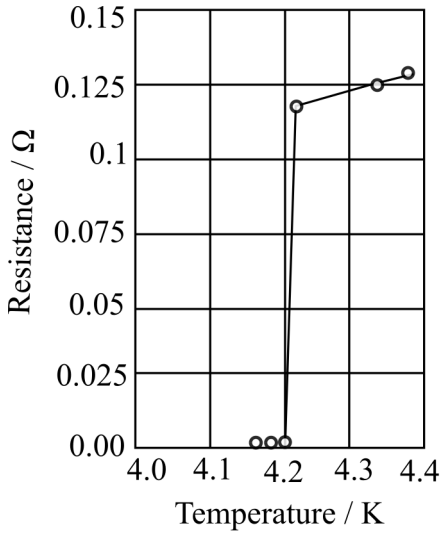


Figure 1.1: Experimental demonstration of mercury superconductivity from Kamerlingh Onnes original research. Adapted from [24].

Kamerlingh Onnes passed a current through a pure mercury wire and measured its resistance as he steadily lowered the temperature. Instead of the resistance levelling at 4.2K it suddenly vanished. Deliberately increasing the electrPlotting the resulting Is (?) RN as a function of the phase for a typical short weak link results in Figure 1.15, where the critical current Ic is taken as the maximum value of the function.on scattering by introducing impurities to the mercury did not effect the observed vanishing of resistance [25]. According to Kamerlingh Onnes *"Mercury passed into a new state, which on account of its extraordinary electrical properties may be called a superconductive state*".

In 1933, Walther Meissner and Robert Ochsenfeld [26] used a single crystal of tin and found it to have an interesting magnetic property of excluding a magnetic field, unlike simply a perfect conductor which would conserve magnetic flux within it. This phenomena of magnetic field expulsion is caused by a current flow that generates a magnetic field inside the superconductor that balances the field that would have otherwise penetrated the material. This is shown in Figure 1.2 and is known as the *Meissner effect*.

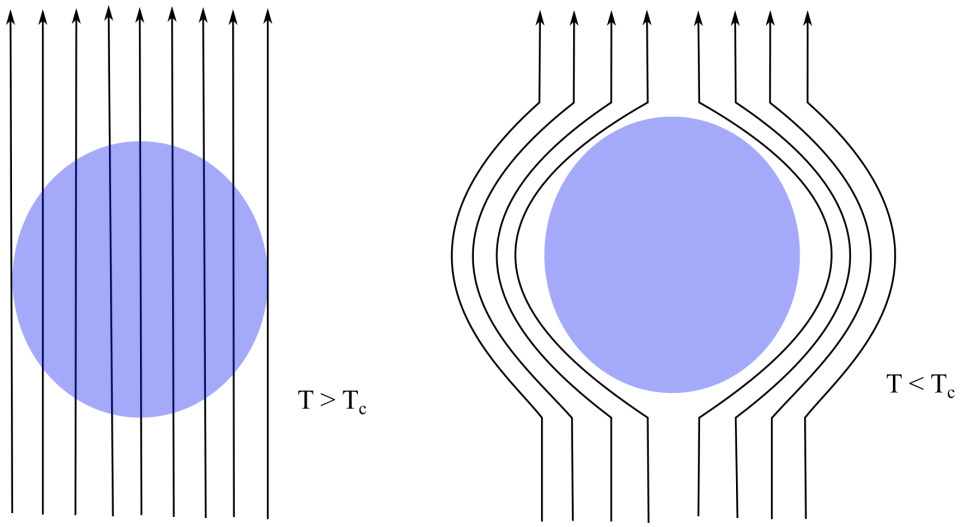


Figure 1.2: Diagram of the Meissner effect. Magnetic field lines, represented as arrows, are excluded from a superconductor when it is below its critical temperature.

Many theories were introduced to examine and describe the nature of supercon-

ductivity, much of the early work relied on phenomenological models. For a more comprehensive look at such a model see ref [27].

London Equations: As a restricted form of the Maxwell equations, the London brothers introduced a set of equations that describe the behaviour of superconductors and are consistent with experimental observation, in particular the Meissner effect:

$$\frac{\partial \mathbf{J}_s}{\partial t} = \frac{n_s e^2}{m}\mathbf{E} \tag{1.1}$$

$$\nabla \times \mathbf{J}_s = \frac{n_s e^2}{m}\mathbf{B} \tag{1.2}$$

It is important to note that these equations did not attempt to explain the microscopic origin of superconductivity. If the second London Equation 1.2 is manipulated by applying Amperes law

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{J}_s$$

then the result is the differential equation

$$\nabla^2 \mathbf{B} = \frac{\mu_0 n_s e^2}{m}\mathbf{B} = \frac{1}{\lambda_L^2}\mathbf{B} \tag{1.3}$$

where λ_{L} is known as the *penetration depth* defined by:

$$\lambda_{\mathrm{L}} = \sqrt{\left(\frac{m}{\mu_0 n_s e^2}\right)} \tag{1.4}$$

Applying Equation 1.3 to a plane boundary located at $x = 0$ we get:

$$B(x) = B(0)e^{-x/\lambda_{\mathrm{L}}} \tag{1.5}$$

which shows the field decaying exponentially over the penetration depth with the magnetic field vanishing in the bulk of the material as shown in Figure 1.3.

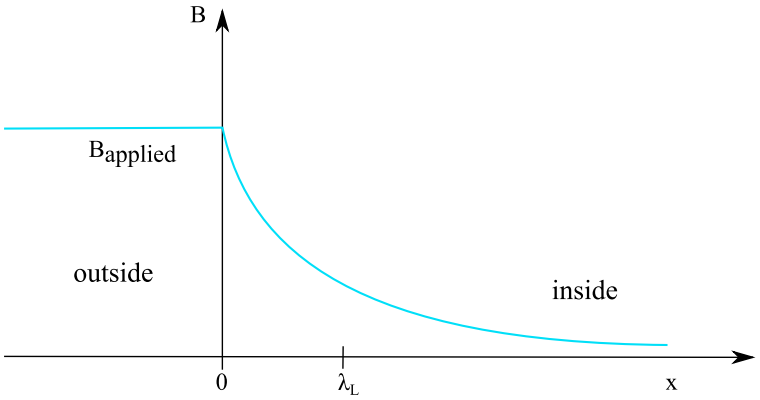


Figure 1.3: Variation of an applied magnetic field inside a superconductor.

At T_c the magnetic field penetrates throughout the material as λ_L diverges. As soon as temperature is lower than T_c the penetration depth goes very close to its value at $T = 0$ establishing the Meissner effect in the bulk of the supwerconductor. Experimentally, the penetration depth often follows the two fluid temperature dependence that has been modelled by Gorter and Casimir [28] as;

$$\lambda(T) = \lambda_L / \sqrt{1 - \left(\frac{T}{T_c}\right)^4} \tag{1.6}$$

Although in theory the penetration depth of most metals should be in the range of 20-50 nm, some measurements showed it to be much longer, by up to one order of magnitude, in some samples of aluminium [29]. This result was only explained by the concept of the coherence length, first introduced by Pippard as the Pippard coherence length ξ_0.

Pippard Coherence Length: Pippard argued that a superconductor should have a characteristic dimension ξ_0 which describes the evolution of the wavefunction or the order parameter of the superconductor over a certain distance. This could be estimated by an uncertainty principle argument

$$\Delta x \gtrsim \hbar/\Delta p \approx \hbar v_F / k T_c \tag{1.7}$$

leading to the definition of a characteristic length

$$\xi_0 = \alpha \frac{\hbar \upsilon_F}{k_{\mathrm{B}} T_{\mathrm{c}}} \tag{1.8}$$

where α is a numerical constant of order unity. ξ_0 plays a role analogous to the mean free path ℓ in the non local electrodynamics of normal metals and were later found to be comparable to the size of a Cooper pair (see BCS theory). Pippard found that he could fit the experimental data on both tin and aluminium by choice of a single parameter $\alpha = 0.15$ [30] in Equation 1.8.

BCS theory: For many years, the phenomenon of superconductivity could not be satisfactorily explained by the laws of conventional physics. However in the early 1950's, American physicists John Bardeen, Leon Cooper, and John Schrieffer [31] formulated a theory for superconductivity that earned them the Nobel Prize in Physics in 1972. According to the BCS theory, interaction between electrons and phonons (the vibrational mode of the positive ions in a crystal lattice) causes a reduction in the coulomb repulsion between electrons, which is sufficient at low temperatures to provide a net long range attraction. This attraction causes the formation of bound pairs of remote electrons of opposite momentum and spin, the so called *Cooper pairs*.

One of the main predictions of the BCS theory is the existence of an energy gap at the Fermi level. In a normal metal the electron states are filled up to the Fermi energy ϵ_F, and there is a finite density of states at the Fermi level $g(\epsilon_F)$. In the BCS theory for superconductors below T_{c}, the electron density of states acquires a small gap separating the occupied and unoccupied states. This gap is fixed at the Fermi energy, and so it does not prevent electrical conduction. A minimum energy of $E_g = 2\Delta(T)$ is required to break a pair, creating two quasi-particle excitations. $\Delta(T)$ was predicted to increase from zero at T_{c} to a limiting value far below T_{c} of

$$E_g(0) = 2\Delta(0) = 3.528 k_{\mathrm{B}} T_{\mathrm{c}} \tag{1.9}$$

The superconducting energy gap close to T_c is

$$2\Delta(T) \approx 3.52 k_B T_c \sqrt{1 - \left(\frac{T}{T_c}\right)} \tag{1.10}$$

where the critical temperature T_c in weakly coupled superconductors can be approximated by:

$$T_c = \frac{1.14\hbar\omega_D}{k_B} e^{-1/N(0)U_{ep}} \tag{1.11}$$

where U_{ep} is the electron-phonon coupling potential and ω_D is the Debye frequency.

Ginzburg-Landau theory: Ginzburg and Landau postulated the existence of an order parameter which characterised the superconducting state [32]. The order parameter is assumed to be some (unspecified) physical quantity which characterises the state of the system. In the normal metallic state above the critical temperature T_c of the superconductor it is zero. While in the superconducting state below T_c it is non zero. Therefore it obeys;

$$\psi(\mathbf{r}) = \begin{cases} 0 & T > T_c \\ \neq 0 & T < T_c \end{cases} \tag{1.12}$$

The order parameter is now usually taken as a measure of the number of superconducting electrons in a system, i.e.

$$n_s = |\psi(\mathbf{r})|^2 \tag{1.13}$$

Close to the critical temperature, T_c, $\psi(\mathbf{r})$ is small enough to apply a Taylor's series expansion to the free energy of the system which is of the form:

$$f = f_{n0} + \alpha|\psi|^2 + \frac{\beta}{2}|\psi|^4 + \frac{1}{2m^*}\left|\left(\frac{\hbar}{i}\nabla - \frac{e^*}{c}\mathbf{A}\right)\psi\right|^2 + \frac{\hbar^2}{8\pi} \tag{1.14}$$

where f_{n0} is the free energy at the normal state. The free energy for the superconducting state and the normal state are respectively f_s and f_n. Their difference $f_s - f_n$ is

$$f_s - f_n = -\frac{H_c^2}{8\pi} = -\frac{\alpha^2}{2\beta} \tag{1.15}$$

The coefficient β is always positive for the theory to hold while there are two different cases for α

$$|\psi|^2 = \begin{cases} \alpha > 0, & T > T_{\mathrm{c}} \\ \alpha < 0, & T < T_{\mathrm{c}} \end{cases} \tag{1.16}$$

- For $T_{\mathrm{c}} < T$, $\alpha > 0$ and f_n reaches its minimum and $|\psi|^2$
- $T_{\mathrm{c}} > T$, $\alpha < 0$ and $|\psi|^2 = -\alpha/\beta$

Using the definition of the thermodynamic critical field H_c, Ginzburg-Landau gave the following expression for the coefficients α and β that are known parameters for a given superconductor:

$$\alpha(T) = -\frac{2e^2}{mc^2} H_c^2(T) \lambda_{eff}^2(T) \tag{1.17}$$

$$\beta(T) = -\frac{16\pi e^2}{m^2 c^2} H_c^2(T) \lambda_{eff}^4(T) \tag{1.18}$$

where

$$\lambda_{eff}^2 = \frac{m^* c^2}{4\pi |\psi|^2 e^{*2}} \tag{1.19}$$

in which e^* and m^* represent the mass and the charge of a Cooper pair i.e. $2e$ and $2m_{\mathrm{e}}$. Moreover, Ginzburg and Landau assumed that the free energy of the superconductor must depend smoothly on the parameter $\psi(\mathbf{r})$. When perturbations such as currents or magnetic fluxes are applied, the system will adopt the wavefunction configuration that minimizes the free energy, leading to a pair of coupled differential equations for $\psi(\mathbf{r})$ and the magnetic vector potential $\mathbf{A}(\mathbf{r})$, which is equal to

$$\beta|\psi|^2\psi + \alpha(T)\psi + \frac{1}{2m^*}\left(\frac{\hbar}{i}\nabla - \frac{e^*}{c}\mathbf{A}\right)^2\psi = 0 \tag{1.20}$$

$$\mathbf{J}_s = \frac{e^*}{m^*}|\psi|^2\left(\hbar\nabla\psi - \frac{e^*}{c}\mathbf{A}\right) \tag{1.21}$$

The result was a generalisation of the London theory to deal with situations in which n_s varies with space, and also to deal with the non-linear response to fields that are strong enough to change n_s.

Ginzburg-Landau Coherence Length: The Ginzburg-Landau equations predict a characteristic "coherence length" $\xi(T)$. Normalisation of the wavefunction using $f = \psi/\psi_\infty$, where $\psi_\infty = -\alpha/\beta$ in the absence of any magnetic field leads to:

$$\frac{\hbar^2}{2m^*|\alpha(T)|}\frac{d^2f}{dx^2} + f - f^3 = 0 \tag{1.22}$$

where

$$\xi^2(T) = \frac{\hbar^2}{2m^*|\alpha(T)|} = \frac{\Phi_0}{2\sqrt{2}H_c(T)\lambda_{eff}} \tag{1.23}$$

The Ginzburg-Landau coherence length should not to be confused with the Pippard coherence length ξ_o since this $\xi(T)$ represents the length scale over which the order parameter Δ or the wavefunction Ψ varies and diverges at T_c, whereas the electrodynamic Pippard's ξ_o is essentially constant for a given superconductor. Using the BCS theory, the expression for the GL coherence length can be approximated for clean limit where $\xi_0 < \ell$

$$\xi(T) = 0.74\frac{\xi_0}{\sqrt{1 - \frac{T}{T_c}}} \tag{1.24}$$

and dirty limit where $\xi_0 > \ell$

$$\xi(T) = 0.855\sqrt{\frac{\xi_0\ell}{1 - \frac{T}{T_c}}} \tag{1.25}$$

1.2 Josephson junctions

Named after the British physicist Brian Josephson [33], Josephson junctions are a subset of weak links; a family of structures that display the Josephson effect. Such structures have an important application in voltage standards [34], quantum-mechanical circuits, such as Superconducting QUantum Interference Devices (SQUIDs) [35], superconducting qubits [36], and RSFQ digital electronics [37]. Different examples of Josephson junctions are shown in Figure 1.4.

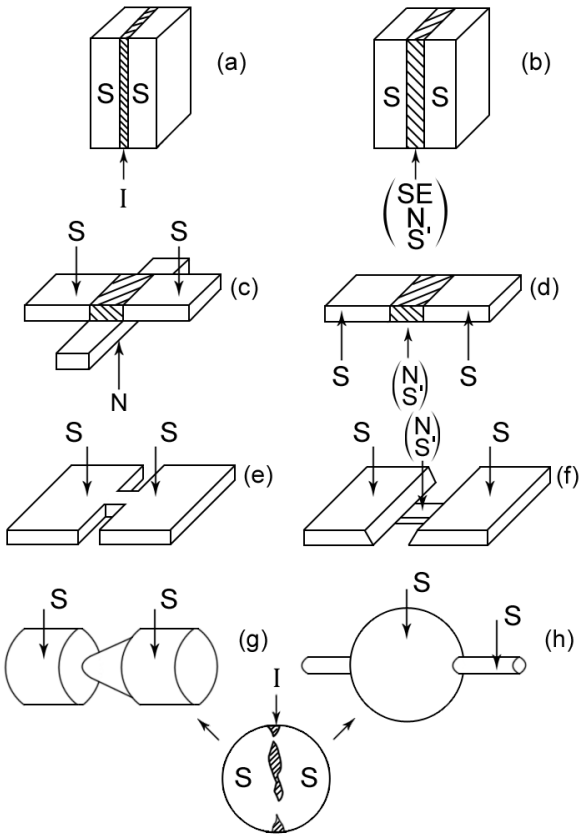


Figure 1.4: Different types of structures where the Josephson effect can take place. (a) tunnel junction, for example, S-I-S sandwich. All others are different weak links (structures with direct non-tunnel-type conductivity): (b) sandwich, (c) proximity effect bridge, (d) ion implanted bridge, (e) Dayem bridge, (f) variable thickness bridge, (g) point contact, (h) blob type junction. S = Superconducting, S' = superconducting with reduced critical parameters, SE = semiconductor (usually highly doped), N = normal metal and I = Insulator. Adapted from Likharev [38]

1.2.1 Josephson effect

Following the BCS theory [31], Gor'kov's derivation of the BCS equations from the Ginzburg-Landau theory [39] and Giaver's current tunnelling experiment across aluminium oxide [40], Josephson wrote a set of equations describing what happens at the interface between two weakly coupled superconductors [41]:

$$I_s = I_c \sin \varphi \tag{1.26}$$

$$\frac{d\varphi}{dt} = \frac{2e}{\hbar} V(t) \tag{1.27}$$

The electrodynamic phenomena taking place at the Josephson Junction are generally divided into stationary (Equation 1.26) and non-stationary (Equation 1.27) effects. Depending on whether the variables, including the phase difference change with time. If the phase $\varphi = \theta_2 - \theta_1$, where θ_1 and θ_2 are the phases of the order parameter Δ in the electrodes, remains constant, the voltage across the junction is zero, at the same time a non-zero super-current as shown by Equation 1.26 can flow through the junction with magnitude $|I_\mathrm{s}| \leqslant I_\mathrm{c}$, where I_c is the critical current. Therefore if the current is not larger than the critical current I_c then there will be no voltage drop across the junction

In Josephson's theory, in the stationary state described as the DC effect, the supercurrent I_s is a sinusoidal function according to Equation 1.26 of the phase. In the absence of fluctuations (see sections 1.2.1) there are two sets of solutions for the stationary state that correspond to $V = 0$:

$$\varphi = \varphi_n = \arcsin\left(I/I_c\right) + 2\pi n \tag{1.28}$$

$$\varphi = \varphi_n^{'} = \pi - \arcsin\left(I/I_c\right) + 2\pi n \tag{1.29}$$

Before Josephson's prediction, it was only known that normal (non-superconducting) electrons could cross an insulating barrier, by means of quantum tunnelling. Josephson was the first to predict the tunnelling of superconducting Cooper pairs [41]. The DC Josephson effect had been seen in experiments prior to 1962, but had been attributed to "super-shorts" or breaches in the insulating barrier leading to the direct conduction of electrons between the superconductors.

Response to DC source (The AC effect): Among the non-stationary (AC) effects occurring when the phase of the junction changes with time, from Equation 1.27, when a Josephson junction experiences a nonzero voltage above I_c the phase grows linearly in time to yield

$$\varphi = \frac{2e}{\hbar}\int V dt = \omega_J t + const \qquad \omega_J = \frac{2e}{\hbar}\overline{V(t)} \tag{1.30}$$

which in turn yields an alternating current $I_s = I_c \sin(\omega_J t)$, that oscillates at the Josephson frequency $f_J = \omega_J/2\pi = V(t)/\Phi_0$. The typical oscillations of the Josephson supercurrent and the voltage can be seen in Figure 1.5.

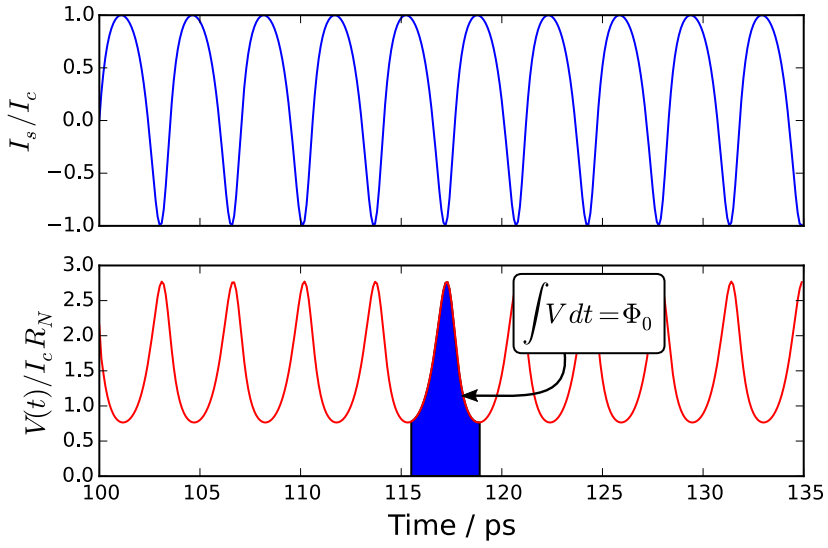


Figure 1.5: Example of the supercurrent I_s oscillations and the corresponding voltage oscillations in a typical Josephson junction. Integrating the voltage curve results in multiple of the flux quanta Φ_0.

Response to AC signal: Once an alternating voltage is applied to a junction so that $V(t) = V_0 + V_{\mathrm{rf}} \cos(\omega_{\mathrm{rf}} t)$, the phase then becomes:

$$\varphi(t) = \varphi_0 + \frac{2\pi V_{\mathrm{dc}} t}{\Phi_0} + \frac{2\pi V_{\mathrm{rf}}}{\Phi_0 \omega_{\mathrm{rf}}} \sin(\omega_{\mathrm{rf}} t) \tag{1.31}$$

Using $\omega_{\mathrm{J,dc}} = 2\pi V_{\mathrm{dc}}/\Phi_0$ and $\omega_{\mathrm{J,rf}} = 2\pi V_{\mathrm{rf}}/\Phi_0$ and substituting this into Equation 1.26 with a Fourier-Bessel series expansion, the supercurrent can be expressed as:

$$I_{\mathrm{s}} = I_{\mathrm{c}} \sum_{-\infty}^{\infty} (-1)^n \mathcal{J}_n \left(\frac{\omega_{\mathrm{J,rf}}}{\omega_{\mathrm{rf}}} \right) \sin\left(\varphi_0 + \omega_{\mathrm{J,dc}} t + n\omega_{\mathrm{J,rf}} t\right) \tag{1.32}$$

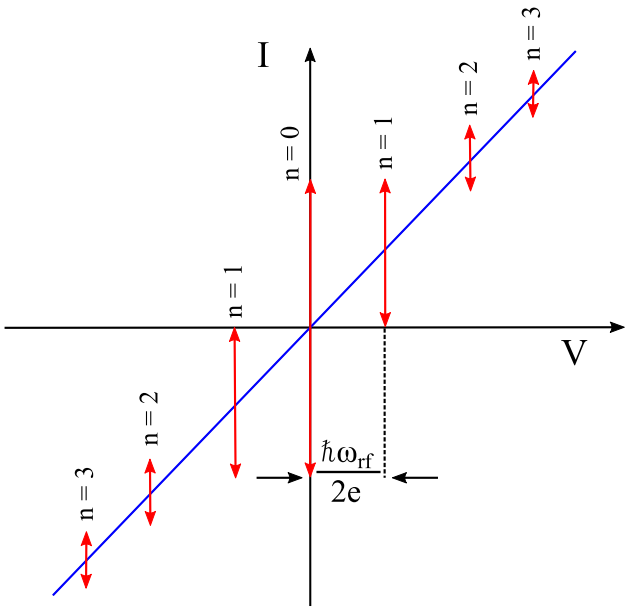


Figure 1.6: The dc component of I_{s} versus the applied dc voltage for a junction biased by a voltage $V(t) = V_0 + V_{\mathrm{rf}} \cos(\omega_{\mathrm{rf}} t)$. Adapted from Enss and Hunklinger [42].

Only in a few situations can the net current in a Josephson junction be approximated by the supercurrent I_{s}, in general other current components have to be taken into account.

Normal (quasiparticle) current $\mathbf{I}_N$: At finite temperatures, thermal breakup of Cooper pairs results in a finite density of normal electron referred to as "quasiparticles". In the zero voltage state the quasiparticles do not contribute to the Josephson current. However if the phase of the junction changes with time according to the Equation 1.27, then the quasiparticles contribute towards the Josephson junctions total current. This current is a resistive current and therefore the voltage state of a Josephson junction is also called the resistive state. At temperature close to T_c the the energy $2\Delta(T)$ required to break up a Cooper pair is much smaller than $k_B T$ resulting in concentration of quasiparticles being close to the electron density in the normal state resulting in current voltage characteristics described by Ohm's law:

$$I_N = \frac{\overline{V(t)}}{R_N} \tag{1.33}$$

Displacement current $\mathbf{I}_D$: When the voltage and its time derivative dV/dt are nonzero due to the change in the electric field, the displacement current I_D plays an important role in total current present in the Josephson junction

$$I_D = C_J \frac{dV}{dt} \tag{1.34}$$

where C_J is the Josephson junction capacitance.

Fluctuation current $\mathbf{I}_F$: The conversation so far about other current components has not taken into account fluctuations that arise due to noise, there are three types of fluctuations, namely **thermal noise**, **shot noise** and $1/f$ **noise**.

(i) Thermal noise: According to the Johnson-Nyqvist formula for thermal noise, when an ohmic resistor satisfies the condition, $k_B T \gg eV, \hbar\omega$, the power spectral density of the current fluctuations in that resistor is described by:

$$S_I(f) = \frac{4k_\mathrm{B}T}{R_\mathrm{N}} \tag{1.35}$$

The relative intensity of the thermal noise current is expressed as ratio of thermal energy and the Josephson junction coupling energy and takes the form of the dimensionless parameter γ:

$$\gamma = \frac{k_{\mathrm{B}}T}{E_J} = \frac{2ek_{\mathrm{B}}T}{\hbar I_{\mathrm{c}}} \tag{1.36}$$

The thermal noise cannot be above E_{J} otherwise the Josephson effect is destroyed it is therefore necessary to have the Josephson coupling energy larger than the thermal energy.

(ii) Shot noise: Once the voltage is large enough that $k_{\mathrm{B}}T, \hbar\omega \ll eV$, then shot noise becomes an important factor. Not to be confused with current fluctuations in equilibrium that occur without any applied voltage as described earlier. Shot noise consists of random current fluctuations due to charge carriers in conductors. The Schottky formula is used to express the power spectral density of these current fluctuations as:

$$S_I(f) = 2eI_{\mathrm{N}} \tag{1.37}$$

and unlike thermal noise fluctuations where the current strength is described by the dimensionless parameter γ, since shot noise follows a Poissonian distribution the strength of the current fluctuations is expressed by the variance of the current I where $\langle I \rangle$ is the current average:

$$\Delta I^2 = \langle (I - \langle I \rangle)^2 \rangle \tag{1.38}$$

(iii) $1/f$ noise: Some times referred to as flicker noise. $1/f$ noise is frequency dependant and is mostly dominant at low frequencies. Typically for Josephson junctions this is below 1kHz and thus can be ignored for many measurements at higher frequencies.

The Resistively and Capacitively Shunted Junction (RCSJ) Model: Using Kirchhoff's circuit law, the net current I flowing through a Josephson junction is expressed as a sum of all current sources leading to $I = I_{\mathrm{s}}+I_{\mathrm{N}}+I_{\mathrm{D}}+I_{\mathrm{F}}$, Expanding this leads to

$$I = I_c \sin\varphi + \frac{V(t)}{R_{\mathrm{N}}} + C_J \frac{dV}{dt} + I_F \tag{1.39}$$

Substituting V in this equation with

$$V(t) = \frac{\Phi_0}{2\pi}\frac{d\varphi}{dt} \tag{1.40}$$

results in the non-linear equation

$$I = I_{\mathrm{c}} \sin\varphi + \frac{\Phi_0}{2\pi R_{\mathrm{N}}}\frac{d\varphi}{dt} + C_{\mathrm{J}}\frac{\Phi_0}{2\pi}\frac{d^2\varphi}{dt^2} + I_{\mathrm{F}} \tag{1.41}$$

Equation 1.41 is more commonly referred to as the Resistively and Capacitively Shunted Junction (RCSJ) model and is used to describe the the net current through a Josephson junctions and is represented in an equivalent circuit diagram as a Josephson junction in parallel with a resistor and a capacitor as shown in Figure 1.7.

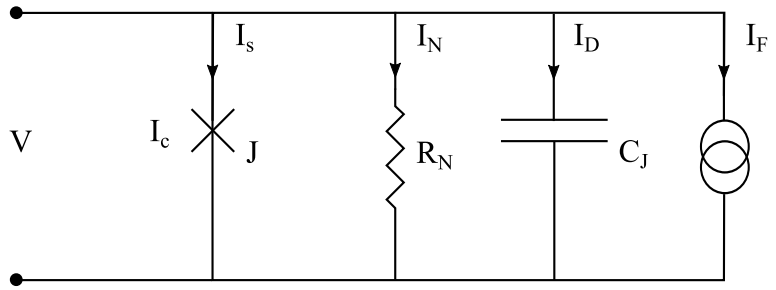


Figure 1.7: Equivalent circuit of the RCSJ model for a real Josephson junction.

As the name suggests the RCSJ model represents an ideal Josephson junction as a junctions in parallel with a a resistor, a capacitor and noise current source. Rewriting Equation 1.41 using the dimensionless parameters τ_J and the Stewart-McCumber parameter β_c, the original equations becomes:

$$\frac{i}{I_c} = \sin\varphi + \frac{d\varphi}{d\tau} + \beta_c \frac{d^2\varphi}{d\tau^2} \tag{1.42}$$

where

$$\tau = \frac{t}{\tau_J} \qquad \tau_J = \frac{\Phi_0}{2\pi}\frac{1}{I_c R_N} \tag{1.43}$$

and

$$\beta_c = \frac{R_N C_J}{\tau_J} = \frac{2\pi I_c R_N^2 C_J}{\Phi_o} \tag{1.44}$$

Depending on the quantitative value of β_c, it is possible to distinguish two limiting types of junctions; overdamped $\beta_c \ll 1$ and underdamped $\beta_c \geqslant 1$.

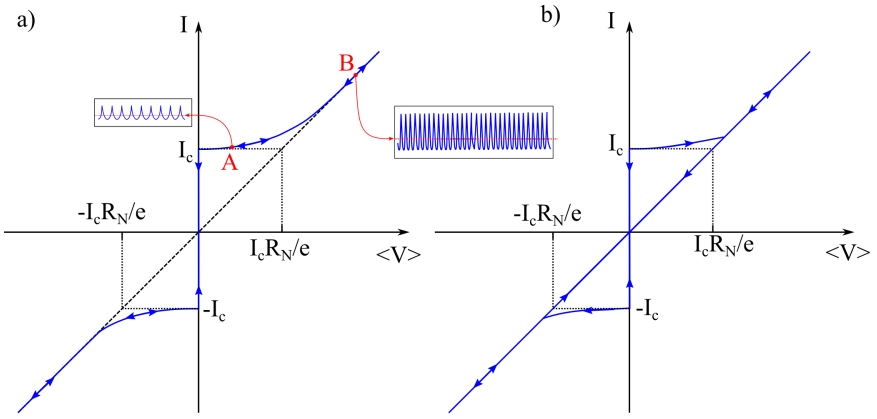


Figure 1.8: (a) Current-voltage characteristics of an overdamped and (b) underdamped Josephson junction. The arrows indicate the direction of the current sweep and the inset plots in (a) demonstrate the time domain voltage oscillations of the Josephson junctions

Overdamped: If $\beta_c \ll 1$ then the weak link is said to be overdamped. The capacitance of the weak link is considered negligible in the electrical circuit. The I-V curve of an overdamped weak link driven by a DC current source in the absence of noise is given by

$$\overline{V(t)} = I_c R_N \sqrt{\left(\frac{I}{I_c}\right)^2 - 1} \tag{1.45}$$

The I-V characteristics are non-hysteretic as shown in Figure 1.8(a) and the Josephson oscillations at different biasing points can be also be seen in the figure.

Underdamped : If $\beta_c \geqslant 1$ the junction is then said to be underdamped and the I-V characteristics become hysteretic as shown in Figure 1.8-(b). This can be explained by the fact that the relaxation constant of the RC components is much greater than the Josephson response, limiting the dynamics of the junction.

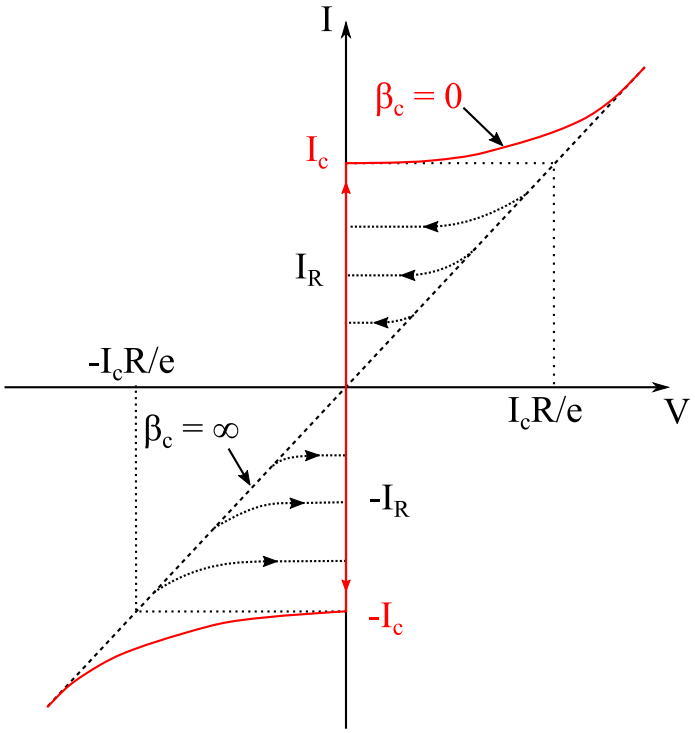


Figure 1.9: RCSJ model current -voltage characteristics at intermediate damping. The arrows mark the return current values I_R at which the junction returns to the zero-voltage state.

Washboard model: Equation 1.41 from the RCSJ model can be written in the form

$$\left(\frac{\hbar}{2e}\right) C\frac{d^2\varphi}{dt^2} + \left(\frac{\hbar}{2e}\right)\frac{1}{R_N}\frac{d\varphi}{dt} + I_\mathrm{c}\left[\sin\varphi - \frac{I}{I_\mathrm{c}} + \frac{I_\mathrm{F}(t)}{Ic}\right] \tag{1.46}$$

Using the Josephson coupling energy $E_\mathrm{J} = \hbar I_\mathrm{c}/2e$, multiplying through by $\hbar/2e$ and normalising the currents to $i = I/I_\mathrm{c}$ and $i_\mathrm{F}(t) = I_\mathrm{F}(t)/I$ results

$$\left(\frac{\hbar}{2e}\right)^2 C\frac{d^2\varphi}{dt^2} + \left(\frac{\hbar}{2e}\right)^2\frac{1}{R_N}\frac{d}{d\varphi}\{E_\mathrm{J}\left[1 - \cos\varphi - i\varphi + i_\mathrm{F}(t)\varphi\right]\} \tag{1.47}$$

Equation 1.47 can be interpreted in the context of a particle moving along the x-axis with mass m and damping η in a potential U. The differential equation describing this particle is

$$m\frac{d^2x}{dt^2} + \eta\frac{dx}{dt} + \frac{dU}{dx} = 0 \tag{1.48}$$

Comparing Equations 1.46 and 1.47 shows the clear relationship between the motion of the phase of a Josephson junction and the motion of a particle of mass m with damping η in potential U as

$$m = \left(\frac{\hbar}{2e}\right)^2 C \qquad \eta = \left(\frac{\hbar}{2e}\right)^2\frac{1}{R_N} \qquad U = E_\mathrm{J}\left[1 - \cos\varphi - i\varphi + i_\mathrm{F}(t)\varphi\right] \tag{1.49}$$

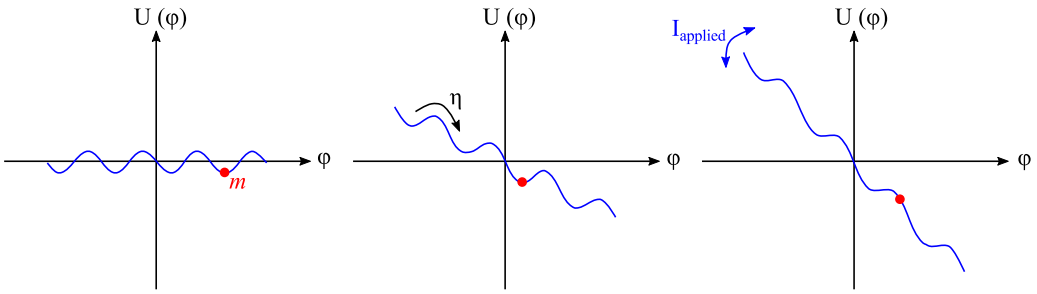


Figure 1.10: The relationship between the damped motion of a particle of mass m and the phase of a Josephson junction in the tilt washboard potential U. The applied current I results in a tilt of the potential U. Graphs represent, zero I_applied, small I_applied and large I_applied respectively.

The washboard model is visualised in Figure 1.10 where the mass of the particle m is proportional to the capacitance of the junctions C, whilst the damping is proportional to $1/R$.

In addition to the effect of β_c, thermal effects also influence the shape of the IV graph, When thermal noise current is included into the RSCJ equation for an overdamped junctions, the relationship stated in Equation 1.45 does not hold any longer. Ambegaokar and Halperin showed that thermal fluctuations result in rounding of the I-V curve due to phase slippage resulting in a non-zero voltage even in the limit $I \to 0$ and in turn resulting in suppression of I_c [43].

Thermal noise and IV rounding: The effect of thermal noise on I-V characteristics of Josephson junction was first modelled in 1969 by Ambegaokar and Halperin [44] by equating the motion of the phase to that of of a Brownian of a particle of mass m in potential U as was seen in the washboard model. Ambegaokar and Halperin formed a Fokker-Planck equation [45] which, when solved derives the solution:

$$v = \frac{4\pi}{\gamma}\left\{(e^{\pi\gamma x}-1)^{-1}\left[\int_0^{2\pi} d\varphi f(\varphi)\right]\left[\int_0^{2\pi} d\varphi' \frac{1}{f(\varphi')}\right] + \int_0^{2\pi} d\varphi \int_0^{2\pi} d\varphi' \frac{f(\varphi)}{f(\varphi')}\right\}^{-1} \tag{1.50}$$

where

$$f(\varphi) = \exp\left(-U(\varphi)/T\right) \tag{1.51}$$

and

$$U(\varphi) = \frac{1}{2}\gamma T\left(i\varphi + \cos\varphi\right) \tag{1.52}$$

A simpler form of Equation 1.50 was introduced by M.S Colclough [46] in the form of:

$$v = \frac{\gamma}{2}\sinh\left(\frac{\pi i}{\gamma}\right)\left[\int_0^{\frac{\pi}{2}} \cosh\left(\frac{2\varphi i}{\gamma}\right)\mathcal{I}_0\left(\frac{2}{\gamma}\cos\varphi\right)d\varphi\right]^{-1} \tag{1.53}$$

where $\mathcal{I}_0$ is the modified Bessel function. Plotting Equation 1.53 at different values of γ results in:

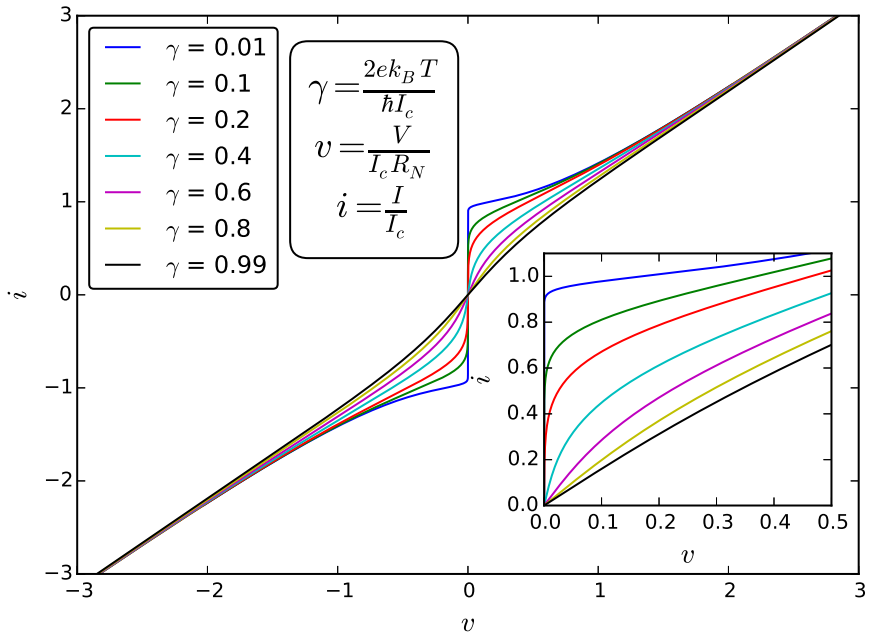


Figure 1.11: Numerical simulations of the I-V graph predicted by Equation 1.53 at different values of γ.

The thermally activated phase slippage can be explained in the context of the washboard model. For current values $I < I_c$ due to thermal activations the particle can escape its local minimum and the phase moves down the tilt washboard potential U resulting in a finite voltage. As γ increases the rounding increases as shown in Figure 1.11.

1.3 Constriction “S-C-S" weak links

Unlike tunnel junctions, where the two superconducting electrodes are separated by a thin insulating barrier and hence are defined by these barriers, constriction weak links on the other hand can be defined by geometry without a barrier. Prominent examples are point contact structures such as that shown in Figure 1.4 (g), or constrictions '*S-C-S*' Figure 1.4 (e) which are of particular importance to this report due fabrication simplicity allowing them to be incorporated into complex integrated circuit chips in very few fabrications steps. As such the following sections will look

at constriction type weak links in more detail.

1.3.1 Critical length L_c and effective length L_{eff}

Unlike other types of junctions the Josephson effect extends into the electrode banks of constriction type weak links, meaning that an effective length L_{eff} rather than the geometric length L which dictates a weak links properties, comparison and classification of such structures therefore focuses on L_{eff} and is compared to characteristic length ξ_{GL} and the mean free path ℓ.

Effective length L_{eff}: Constriction weak links with $L_{\text{eff}} \ll \xi_{\text{GL}}$ are denoted as *short* or *dirty* to distinguish them from *long* or *clean* weak links for which $L_{\text{eff}} \gtrsim \xi_{\text{GL}}$. The terms *dirty* and *clean* for constriction weak links are not to be confused with the well known dirty and clean limits in the general theory of superconductivity, where they are used to denote the relation between values of ℓ and the coherence length ξ_0. The order parameter variation extends into the banks, involving them in the nonlinear Josephson effect. Based on the assumption that the effects extends over a length δ into the banks, Likharev postulated a one-dimensional superconducting electrodes in equilibrium (ODSEE) model for the structure with effective length $L_{\text{eff}} = L + 2\delta$ as shown in Figure 1.12.

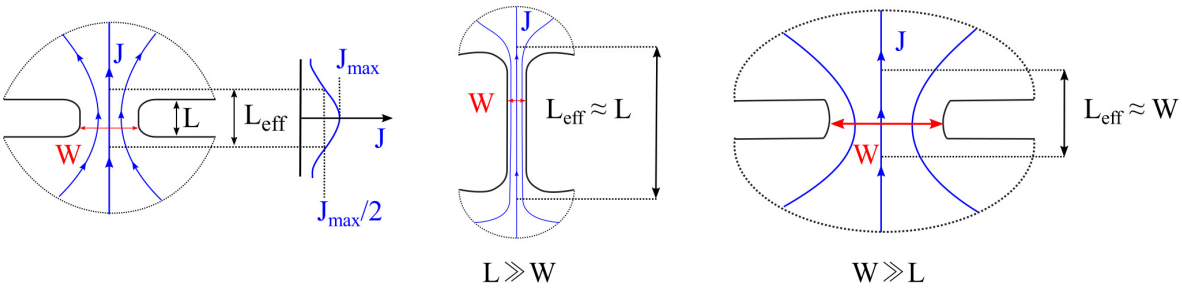


Figure 1.12: Current density for constriction weak links with various geometrical lengths L and widths W . The current density falls off to half its maximum value at $L_{\text{eff}} = \max(\text{L}, \text{W})$. Adapted from Likharev and Yakobson [47].

Critical length L_c: Numerical simulations of the Usadel equations performed by Likharev and Yakobson [47] demonstrate that at L > 3.5$\xi(T)$, the current phase relation becomes multivalued as shown in Figure 1.13.

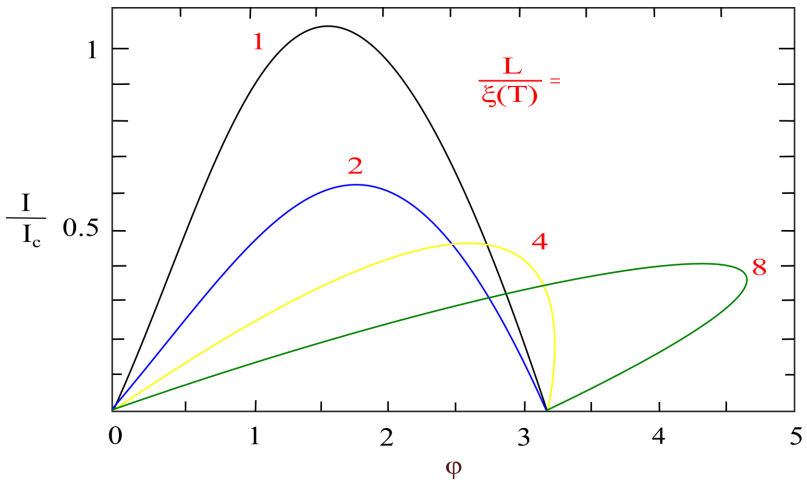


Figure 1.13: The current phase relation for nanobridges of different length ratio L/ξ(T). Current is normalised to the critical current I_0. Adapted from Likharev [38].

This deviation from ideality occurs at values $L > L_c$ where $L_c \approx 3.5\ \xi(T)$. In this region the current phase relationship becomes multivalued and the constriction weak link no longer exhibits the ideal Josephson effect, this limiting length is called the critical length L_c. In addition to the existence of L_c, further simulations by Likharev and Yakobson identified two additional regions that depend not on L_c but on a critical width W_c. In the region $W < W_c$ where $W_c \approx 4.44\ \xi(T)$, phase slippage results in 1D-depairing, whilst for $W > W_c$ coherent vortex motion ensures long range order. This is shown in Figure 1.14.

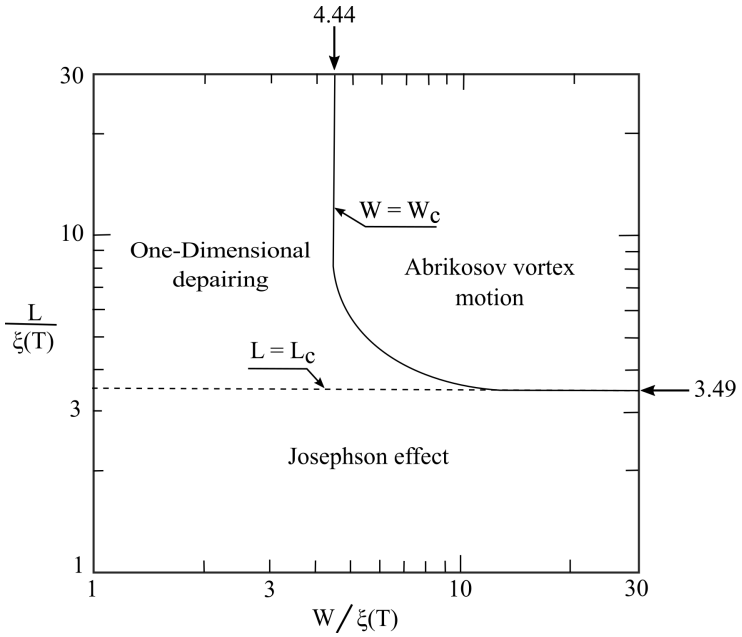


Figure 1.14: The effect of L and W normalised to $\xi(T)$ on the current phase relation. Adapted from Likharev [38].

1.3.2 Critical current

Although developed for tunnel junctions, the Josephson theory can be extended to constriction weak links as a good approximation assuming the dimensions are comparable to the Ginzburg-Landau coherence length ξ_{GL}.

Ambegaokar and Baratoff (AB) model: Weak links of the constriction type "*S,C,S*" have been analysed within the framework of the Ginzburg-Landau theory by Ambegaokar and Baratoff [48] and then by Aslamazov and Larkin [49] at temperatures close to T_{c} where the properties of the bridge coincide in the main with properties of Josephson tunnel junctions which satisfy

$$I_s(\varphi)R_n = \frac{\pi\Delta}{2e}\tanh\left(\frac{\Delta}{2k_{\mathrm{B}}T}\right) \tag{1.54}$$

Equation 1.54 holds well at temperatures close to T_{c}, but as temperatures move away from T_{c} it becomes a very poor fit. In 1975 and 1977, Kulik and Omelyanchuk developed an alternative set of equations that better model the effect of temperature

on I_c of different weak links.

KO(I): The first case(denoted as (KO-I)) [38] applies to *dirty* or *short* weak links and gives

$$I_s(\varphi)R_n = \frac{2\pi k_B T}{e} \sum_{\omega>0} \frac{2\Delta\cos(\varphi/2)}{\delta} \arctan\frac{\Delta\sin(\varphi/2)}{\delta} \tag{1.55}$$

where $\delta = \sqrt{\Delta^2\cos^2(\varphi/2) + (\hbar\omega)^2}$ [1]and the n^{th} Matsubara frequency $\hbar\omega$ satisfies $\hbar\omega = \pi k_B T(2n+1)$ where n is a positive integer. Plotting the resulting $I_s(\varphi)R_N$ as a function of the phase for a typical short weak link results in Figure 1.15, where the critical current I_c is taken as the maximum value of the function.

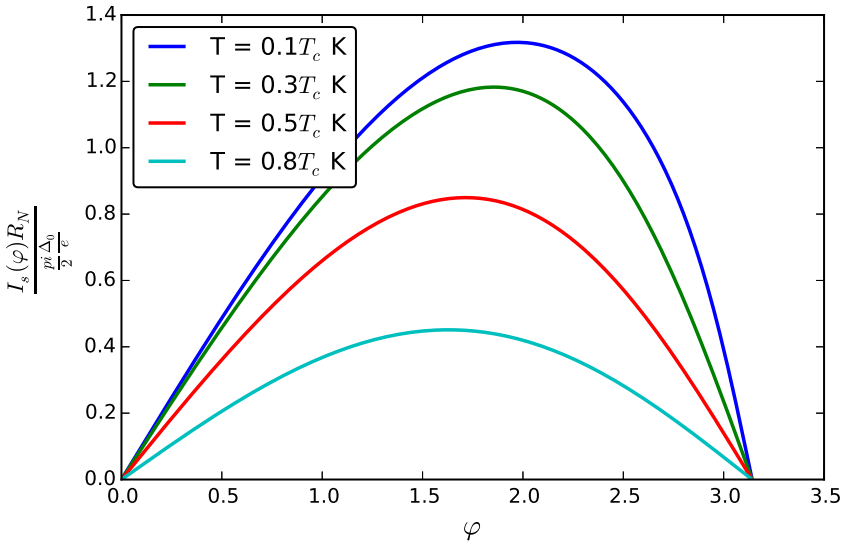


Figure 1.15: $I_s(\varphi)$ relationship for a typical short Nb weak link produced from the KO(I) equations, $I_s(\varphi)$ tends from a sinusoidal to a non-sinusoidal relation as $T \to 0$. I_c is taken as the maximum value of the function.

KO(II): The second case(KO-II) [50] applies to *clean* or *long* weak links and gives

$$I_s(\varphi)R_N = \frac{\pi\Delta}{e}\sin(\varphi/2)\tanh\frac{\Delta\cos(\varphi/2)}{2k_B T} \tag{1.56}$$

[1]not to be confused with the δ from the ODSEE model encountered earlier.

Plotting the $I_{\mathrm{s}}(\varphi)R_{\mathrm{N}}$ in this region gives the behaviour shown in Figure 1.16

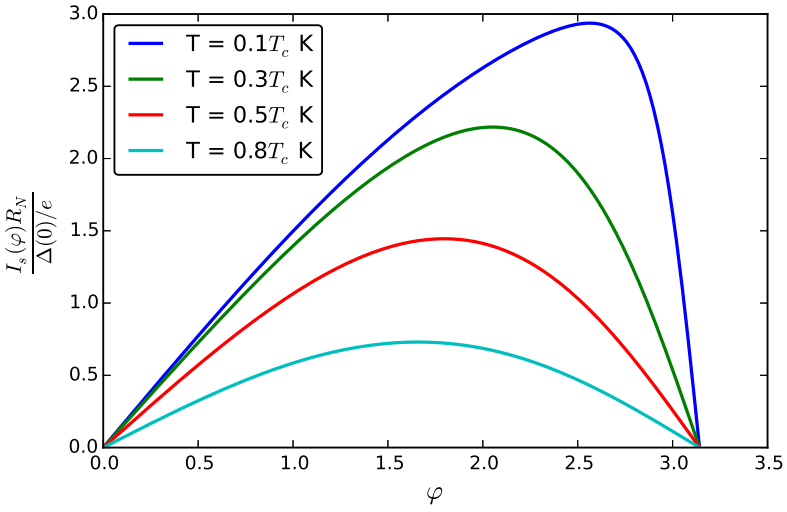


Figure 1.16: $I_{\mathrm{s}}(\varphi)$ relationship for a typical long/clean weak link produced from the KO(II) equations, as with the KO(I) theory, $I_{\mathrm{s}}(\varphi)$ tends from a sinusoidal to a non-sinusoidal relation as $T \to 0$.

Considering the maximum of Equations 1.54, 1.55, 1.56, a graphical representation of the the temperature dependence of I_{c} can be produced for each case as shown in Figure 1.17.

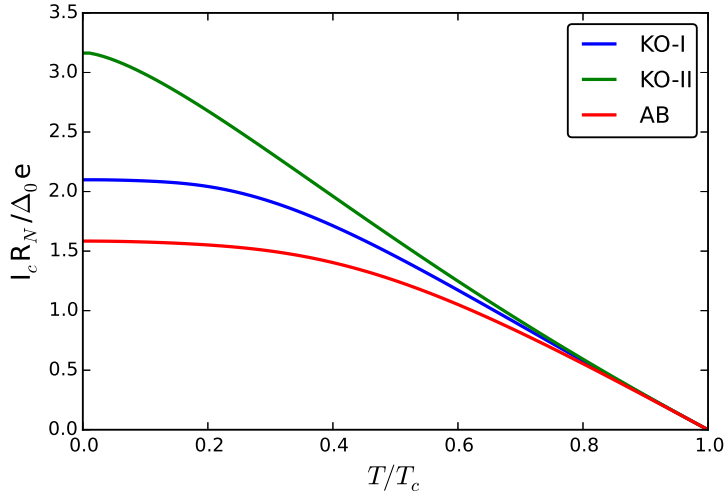


Figure 1.17: Graphical representation of the KO-I, KO-II and the AB predictions for the temperature dependence of $I_{\mathrm{c}}R_{\mathrm{N}}$.

It is in short weak links where the *ideal* Josephson effect is observed since the I_s relationship has a close to perfect sinusoidal relation to the phase as shown in Figure 1.16, and an increase in the effective length causes considerable deviation from the ideality. However, the details may differ depending on the mean free path ℓ.

1.4 Voltage standards

1.4.1 DC voltage standard

The most significant metrological application of superconductivity and especially the Josephson effect is the Josephson DC voltage standard. This quantum standard enables the reference of the unit of voltage just to physical constants, and is used in many laboratories world wide for high precision voltage measurements.

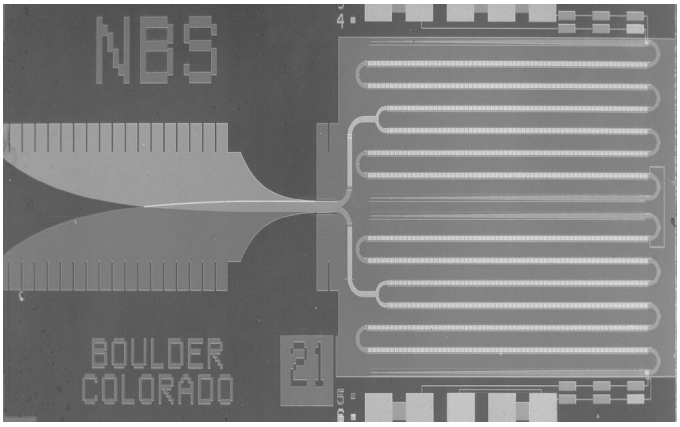


Figure 1.18: One-volt NIST Josephson Junction array standard having 3020 junctions. Microwave energy is fed to four chains of junctions through the fine guide structure at the left. The thin tapered structures at the end of each chain are terminations to prevent reflection of energy back up the chain [51].

The Josephson effect reduces the reproduction of voltages to the determination of a frequency, which can be finely controlled with high precision and accurately referenced to atomic clocks. As will be seen in Chapter 2 this follows from

$$V = \frac{h}{2e} f = \Phi_0 f \tag{1.57}$$

The inverse of the flux quantum, $1/\Phi_0$, is called the Josephson constant, and is denoted K_J. In 1990 the adopted value was $K_{J-90} = 483598 \times 10^9$Hz/V. A single Nb tunnel junction operated at the first-order constant-voltage step generates about 145μV, when irradiated by 70 GHz microwaves [52]. Highly integrated junction series arrays are therefore needed to achieve practical output voltages up to 1 V or 10 V [53].

1.4.2 AC voltage standard background

The Josephson effect may be applied to synthesise an AC waveform with metrological accuracy, aiming at the AC voltage standard or precision AC measurements. Most of the research towards an AC voltage standard revolves around employing fast Digital to Analogue (D/A) converters as means of exploiting the Josephson effect and in particular flux quantisation as means of achieving AC voltage standards. There are three different approaches that exploit the principle of D/A converters to achieve the AC voltage standard:

- Binary
- Pulse driven
- RSFQ

Binary voltage standard: DC voltage standards based on hysteretic Josephson junctions cannot change the voltage with the speed fast enough to generate an AC waveform even at a frequency as low as a few Hz. The first successful approach to realise a rapidly programmable DC voltage standard was the *Binary-type* Josephson D/A converters proposed by NIST [54]. In this approach, an array of nonhysteretic junctions is divided into sections containing a binary number of junctions (1,2, ... 2n). The output voltage is given as $V = Nf/K_J$, where N is the number of digitally programmable voltage steps N and K_J is the Josephson constant. Different output voltages are programmed by using independent bias

currents to select an arbitrary number of voltage steps N and therefore the voltage of each array segment in the binary series can be controlled,

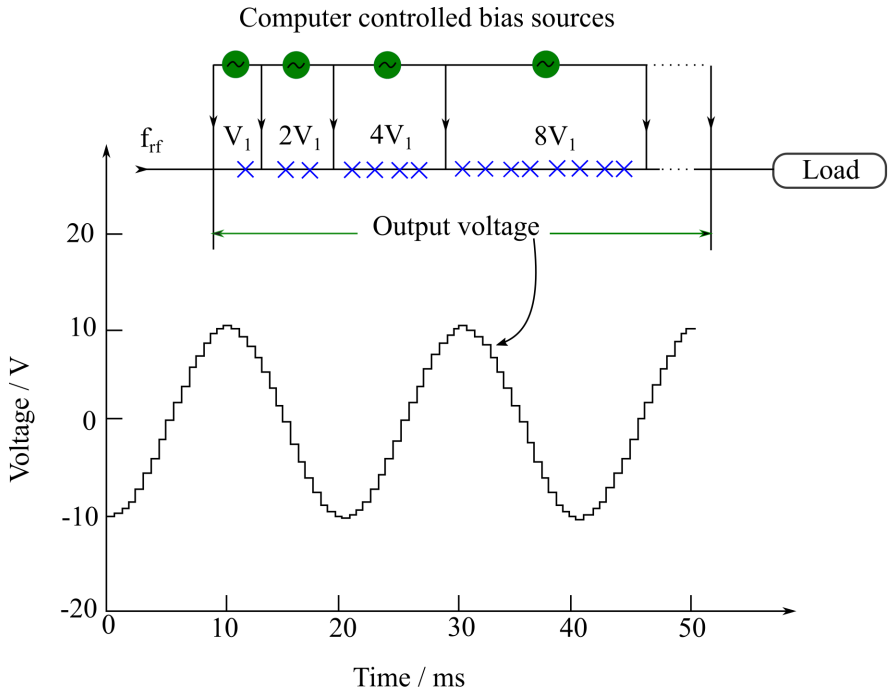


Figure 1.19: Circuit schematic of a programmable Josephson Voltage Standard (Binary voltage standard) and the resultant voltage output where the voltage steps are clearly visible and produce a AC output.

Tri-layer tunnel junctions with large critical currents have been developed by NIST to provide higher output current and better stability against noise [55]. Their over damped characteristic results in a nonhysteretic I-V curve that is inherently stable without the use of external shunt resistors. This junction technology and circuit design has advanced to the level where a binary sequence circuit with 32768 SNS junctions in nine independently selectable arrays on a single chip has demonstrated stable accurate voltages up to 1.2 V [56]. However, the binary type D/A converter suffers from substantial uncertainty as a result of switching transients and jitters. This is due to the fact that the transitions from one voltage level to another are controlled by external semiconductor circuits. The only way to completely avoid transients at all is to use the so-called pulse driven Josephson arbitrary waveform synthesiser in which the output voltage is controlled not by

changing the total voltage steps N, but by changing the driving frequency f using a microwave digital pulse generator.

Pulse driven voltage standard The interest in quantum-accurate AC waveform synthesis led to the development of another version of Josephson voltage standards for AC applications [57, 58]. The limitations of binary-type D/A converters do not appear, if Josephson junctions are operated by a train of short current pulses. The train of pulses determines the number of flux quanta transferred through the Josephson junctions or weak link at any time [59]. The waveform to be generated is encoded in the pulse train. A high pulse repetition rate generates high voltages; the voltage decreases with decreasing pulse repetition rate. Figure 1.20 schematically shows the principle of operation. The pulse train is typically created by the use of second-order sigma-delta (SD) modulation [60].

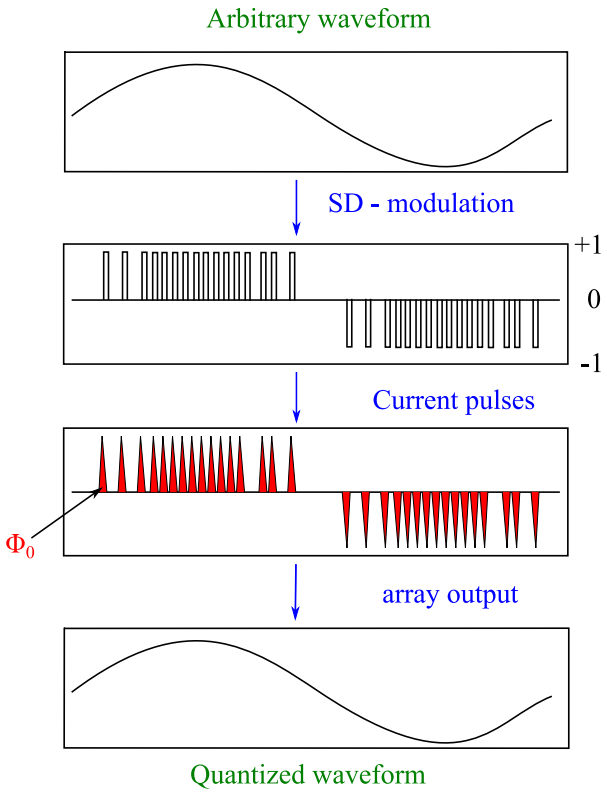


Figure 1.20: Example of a pulse driven voltage standard set-up.

Important steps towards increasing precision and accuracy of pulse drive wave-

form synthesiser involved the development of a code generator allowing a pulse repetition frequency of about 10 GHz [61] and the use of a bipolar drive signal [62, 63]. Overdamped Josephson junctions are embedded into the middle of a coplanar waveguide transmission line (CPW). As the pulses consist of broadband frequency components ranging from DC to about 30 GHz [64], a coaxial microwave assembly is required in order to enable the transmission of these broadband signals.

The broadband pulse drive including DC and low-frequency components causes additional requirements in operation compared to sinusoidal driven arrays. The DC component must be delivered to the array, e.g. by a direct connection to the code generator [65]. A resistive microwave termination at the end of the CPW would produce an unwanted common mode voltage; in order to avoid this common mode voltage, the initially used arrays were designed as lumped elements, whose junction series array are directly grounded. Finally, a simple splitting of the array in parallel microwave paths is not possible [66]. A comparison between the output voltages of a pulse-driven and a binary divided Josephson voltage standard at 8 mV showed an excellent agreement of both systems within a relative deviation of 5×10^{-7} [60, 67].

In both previous examples the underlining principle of single flux quantum manipulation is the core foundation of exploited towards achieving AC voltage standard. However in the binary type voltage standards, the quantised pulses are not counted or monitored through the system and when the system is switched off and on again results in a loss of precision. Pulse driven standards overcome this obstacle since pulses are counted, however complex semiconductor circuitry in the pulse pattern generator means that this is an expensive solution. This can be overcome if the pulse pattern generator can be encoded into the superconducting circuitry, here is where Rapid Single Flux Quantum (RSFQ) technology plays an important role.

1.4.3 Rapid Single Flux Quantum (RSFQ)

In electronics, rapid single flux quantum (RSFQ) is a digital electronics technology that uses superconducting devices, namely Josephson junctions, to process digital signals. RSFQ provides an intrinsic digital coding which represents information by the presence or absence of a magnetic flux quantum $\Phi_0 = h/2e$ in a superconducting loop containing one or more weak links. The presence of a single flux quantum (SFQ) corresponds to a circulating current $J = \Phi_0/L$ in the loop where L is the loop inductance. The exchange of flux quanta between these loops is performed by switching events of the weak links. RSFQ electronics provide very high switching speed in combination with very low power consumption and is a promising field for fast A/D conversion. This technology eliminates the issues that arise from pulse driven AC voltage standards. In this thesis we will investigate whether in combination with constriction type weak links a whole RSFQ circuit can be fabricated on a single chip in one e-beam lithography and metal deposition session.

(i) Background: In RSFQ technology, information is represented as short pulses with a duration of the order Φ_0/I_cR_N. In general it is desirable to use junctions with high I_cR_N to maximise the speed of the device. For a typical I_cR_N product of 1 mV for low temperature superconducting material like Nb the pulse duration is $\approx$ 2 ps. During a single pulse the phase difference across a Josephson junction evolves by 2π and according to the second Josephson equation $V = (\hbar/2e)(d\varphi/dt)$, a 2π change results in voltage pulse of fixed area $\int V dt = \int(\hbar/2e)d\varphi = (\hbar/2e) = \Phi_0 = 2.07 \times 10^{-15}$ Wb.

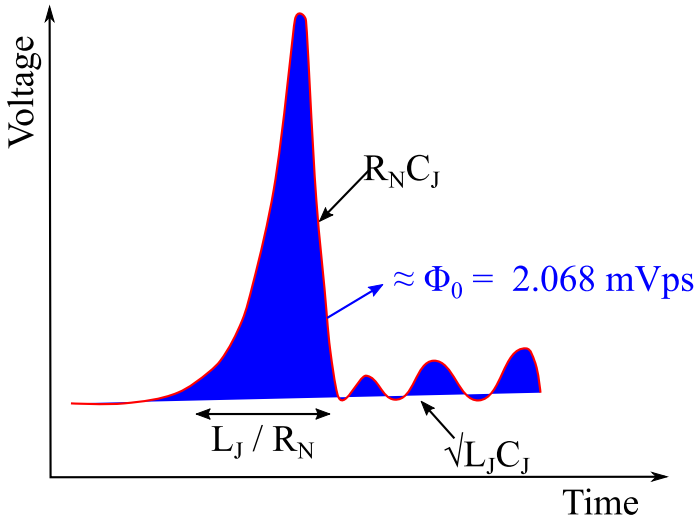


Figure 1.21: A typical voltage pulse. A combination different time dictate the shape of the voltage pulse. The L_J/R_N time constant is responsible for the width/duration of the voltage pulse whilst the R_NC_J time constant is responsible for the duration of the fall of the pulse. Lastly the $\sqrt{L_JC_J}$ time constant determines the length and duration of the tail of the pulse.

The idea of the RSFQ logic is to use these quantised pulses for the storage and transfer of information at GHz speeds without any losses.

(ii) Building blocks: RSFQ circuity can be broken down into four different section as shown in Figure 1.22.

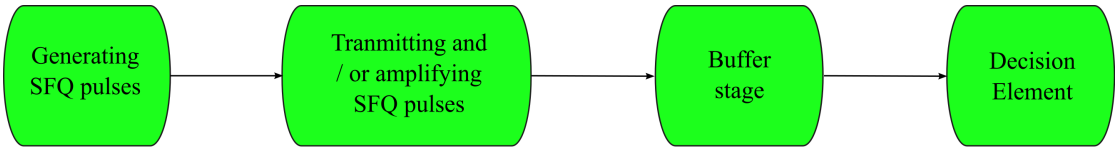


Figure 1.22: Schematic representation of RSFQ circuitry.

The first component of any RSFQ logic circuit is the Single Flux Quantum pulse (SFQ) spike. In principle, the SFQ pulse can be generated through biasing an overdamped Josephson junction slightly above its critical current I_c. This results in a supercurrent I_s flowing in the form of short pulses across the junction with a corresponding voltage pulse of area $\int V dt = \Phi_0$ as shown in Figure 1.23.

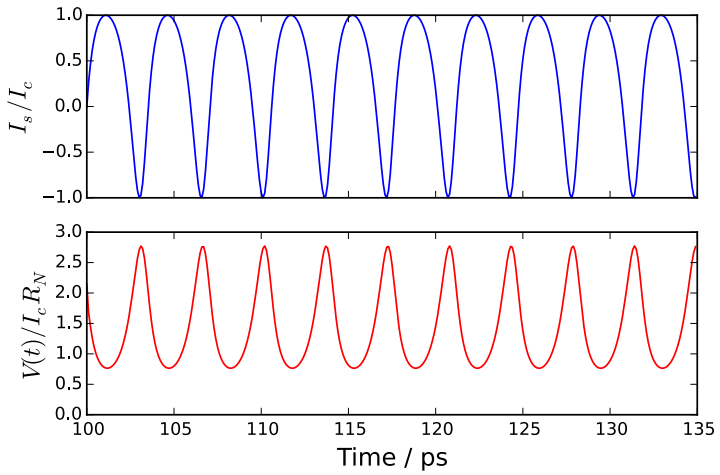


Figure 1.23: Example of time domain supercurrent and voltage oscillation in a Josephson junctions.

(iii) Josephson Transmission Line (JTL): The second stage of an RSFQ logic circuit acts as driver and receiver for transfer of SFQ pulses along a passive superconducting micro-strip line usually referred to as a Josephson Transmission Line (JTL).

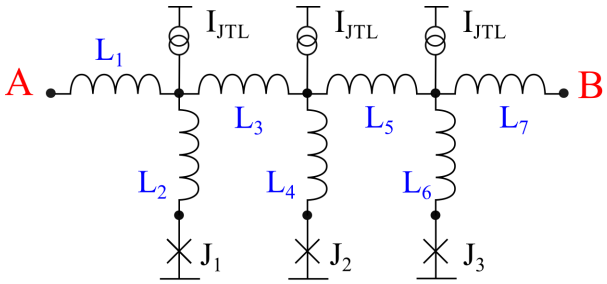


Figure 1.24: Discrete Josephson transmission line for active SFQ pulse transfer.

The JTL consists of several Josephson junctions connected in parallel by superconducting strips of a relatively low inductance, and DC-current biased to their sub-critical state ($I_{\mathrm{JTL}} \lesssim I_{\mathrm{c}}$). The loop inductances are chosen so that the screening current $\beta_{\mathrm{L}} = 2LI_{\mathrm{c}}/\Phi_0$ is just less than unity, so the loops transmit rather than store flux. The Josephson transmission line is a key component of any RSFQ circuitry and tends to be the first element designed and implemented when attempting to fabricate RSFQ circuits. As an SFQ pulse arrives at the JTL a 2π jump of

the Josephson phase is triggered in the first junction of the JTL since the pulse is sufficient for the junction current to exceed I_c. This results in an SFQ pulse developing which in turn triggers a 2π phase shift in the adjacent junction. In effect this is equivalent to a flux quanta moving from left to right across the JTL by the input signal. JTLs can also be used to amplify SFQ pulses. For that, the critical currents of the junctions and the corresponding DC bias currents should grow in the direction of the pulse propagation, with a proportional decrease of the inductances. Unfortunately JTL's transmit pulses equally well in both directions and cannot be used for isolation. A buffer stage is needed as shown in Figure 1.25.

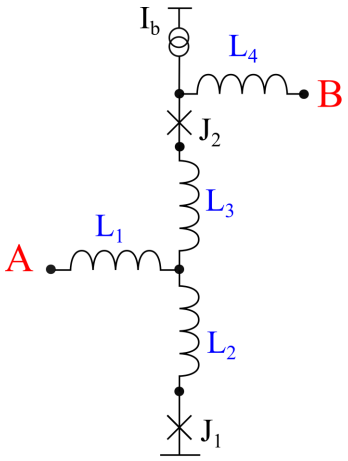


Figure 1.25: buffer stage.

The Buffer stage: The junctions are DC-current biased below their critical currents. If a short pulse arrives at A, it induces a 2π switching of the Josephson phase of junction J_1. This switching produces the standard SFQ pulse at the output terminal B. On the other hand, if the pulse arrives at terminal B, junction J_2 generates a 2π change maintaining an overall zero flux state of the loop. Thus, no SFQ pulse passes to the input A of the circuit, hence it performs the function of a one-directional buffer.

If the DC bias current I_b is not too far from the junction critical current I_c, this SFQ pulse can be triggered by an incoming short pulse, with either the nominal or a somewhat different amplitude. It means that the circuit shown in Figure 1.25

can reproduce SFQ pulses, bringing their area $\int V(t)dt$ to the nominal value Φ_0, providing a moderate voltage gain if necessary.

Josephson Comparator: The Josephson comparator is one of the fundamental building blocks of RSFQ electronics and is the basic decision element for very fast A/D converters, within the RSFQ circuit family it is the exclusive device which provides logical data processing. The behaviour of a Josephson comparator is influenced by the characteristics of the comparator loop and weak links that act as the Josephson elements in the device. This behaviour in turn is dictated by:

- The I_cR_n product of the weak links
- The size of the current biasing of the weak link relative to their critical current
- The loop inductance
- The value of the Stewart-McCumber parameter β_c

A Josephson comparator acts as a sampler, where an SFQ clock input arrives at point A in Figure 1.26 and sets the sampling rate of the two Josephson junctions J_1 and J_2,. Depending on the size of the signal current I_{signal} to be sampled, either one of junctions J_1 or J_2 switch producing a logical "1" output whilst the the other junction remains in the non-active state with an output of "0". In the example shown in Figure 1.26 as the SFQ pulses arrive at point A, they cause junction J_1 to switch and produce voltage pulses up to a certain threshold current (denoted I_{th}). Above this threshold current junction J_2 is triggered and begins producing voltage pulses whereas J_1 reverts to the resting state.

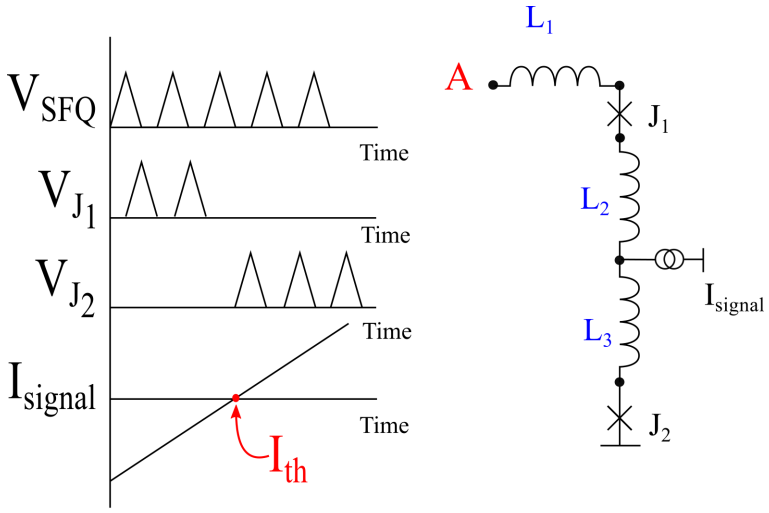


Figure 1.26: Schematic circuit of a typical Josephson comparator setup and the associated output voltage of the different junctions. As an SFQ pulses arrives from point A it triggers junctions J_1 causing it produce voltage pulses up to a threshold I_{signal} value above which J_2 is the junction triggered and produces pulses. This threshold current is denoted as I_{th}.

By either (i) tracking the number of pulses generated from both junctions J_1 and J_2 as a ratio of the incoming pulses generated or (ii) measuring the DC average voltage output from both junctions and dividing by the DC average voltage of the incoming pulses, a switching probability graph can be produced as shown in Figure 1.27 where the transition from "0" to "1" switching probability is represented as a Heaviside step function. In an ideal scenario this transition is a single vertical step as shown in Figure 1.27, however due to the presence of thermal noise in a real device results in a smearing of this step and an uncertainty region where both junctions J_1 and J_2 cab switch. It is this region that is a major limiting factor in device performance and is referred to as the grey zone width.

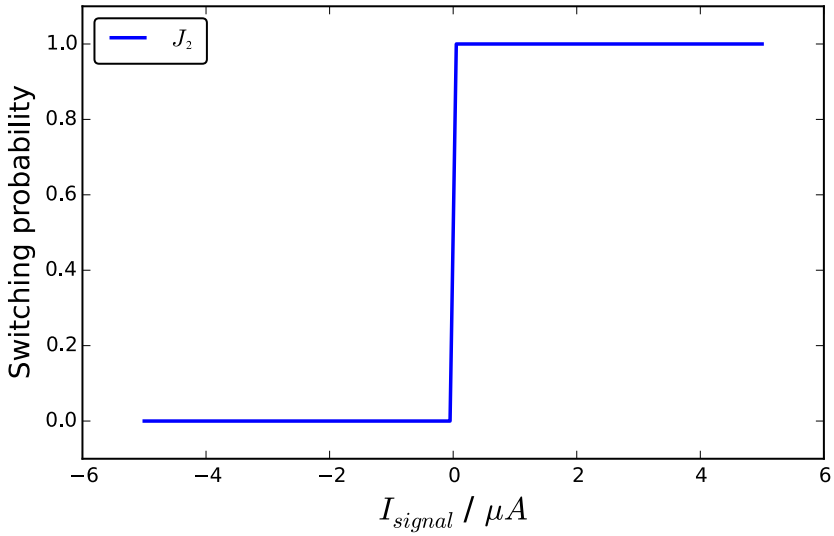


Figure 1.27: Illustrative graph of an ideal switching probability of junction J_2 from Figure 1.26, where the transition from "0" to "1" in the switching occurs as a vertical Heaviside step function.

Chapter 2

Literature review of RSFQ and Josephson comparator devices for high speed circuitry

One of the earliest attempts at utilising the Josephson effect in integrated circuit came from the IBM project to create the worlds first Josephson junction based computer [68]. During the program's lifetime major advances were seen in the development of essential computer components such as logic and memory circuits as shown in Figure 2.1, together with fabrication and packing technologies for such devices. This was seen as the first sign of the march of superconducting integrated circuits based on Josephson junctions and the Josephson effect on the semiconductor circuitry sector. The programme however was stopped in 1983, due to difficulties controlling the I_c spread of Pb-alloy based Josephson junctions and its poor resilience to repeated thermal cycles. Both of these issues were solved with the introduction of Nb based fabrication technologies such as those developed by the "Japanese High speed Computer Project" [1] which resulted in the fabrication of

[1]The Japanese High speed Computer Project was a collaboration between Japanese computer companies and government agencies (ETL, NEC, Hitachi, Fujitsu, NTT)

$Nb/Al_2O_3/Nb$ tunnel junctions which offer higher degrees of controlling I_c spreads when compared to the Pb-alloys [69–71] which allowed large scale integration complexity and is able to better withstand repeated thermal cycling.

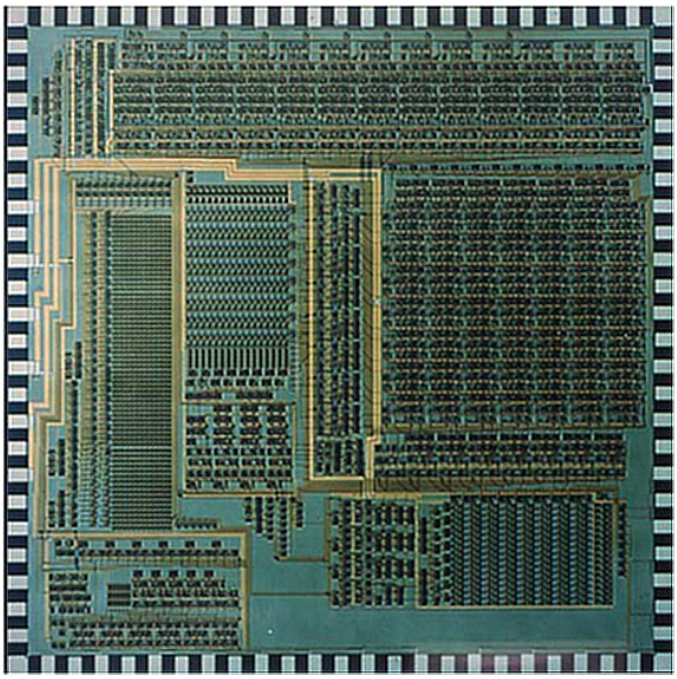


Figure 2.1: Optical image of a Josephson processor developed by IBM. Adapted from W. Anacker [68].

In addition to issues described earlier, IBM's use of underdamped Josephson junctions in a technology referred to as latching logic, where operation of such devices is similar to that of RSFQ circuits and is based on the voltage logical states of "1" and "0" i.e. the zero and finite voltage states that occur for current values between I_c and I_R as seen in Figure 1.8 resulted in clock speeds of less than 1 GHz. This was overcome by the development and introduction of Rapid Single Flux Quantum (RSFQ) logic.

2.1 RSFQ and the Josephson comparator

This was first proposed by Likharev, Semenov and Mukhanov in 1985 as a joint project between Moscow state university (MSU) and Institute of Radioengeneering and Electronics (IRE) [72]. Based on underdamped Josephson junctions, RSFQ circuits utilise flux quantisation to store and transfer information along a circuit. Low power and energy dissipation, and very high speeds are some of the major advantages of RSFQ logic.

2.1.1 RSFQ family

Expanding on the introduction of RSFQ provided in section 1.4.3, In the following section I will briefly describe a few branches of RSFQ logic circuits in terms of high speed devices. The first of such are known are asynchronous components.

Asynchronous Components: Are responsible for the transfer of SFQ pulses across an RSFQ circuit, such example include JTL introduced in section 1.4.3, Splitters and Mergers, examples of such circuits are shown in Figure 2.2. As with the (JTL) introduced in previous chapter the main role of asynchronous components is the transfer of SFQ pulses from an SFQ converter/generator to the main decision making element of an RSFQ circuit the Josephson comparator (see Section 2.2)

Logic gates: The first RSFQ circuits developed by Likharev *et al.* [72] was a logic gate T Flip-Flop circuit shown in Figure 2.2. As with semiconductor circuits RSFQ Logic gates have been developed with logic elements such as AND and OR as shown in Figure 2.2 (d)-(e)

Converters: Are responsible for the conversion of DC currents and pulses into SFQ pulses (DC/SFQ) and vice versa (SFQ/DC). They can take the shape of a single junction or a much more complex arrangement involving several SQUIDs[2] examples of a DC/SFQ circuit is shown in Figure 2.2 (g)

[2]Superconducting QUantum Interference Devices

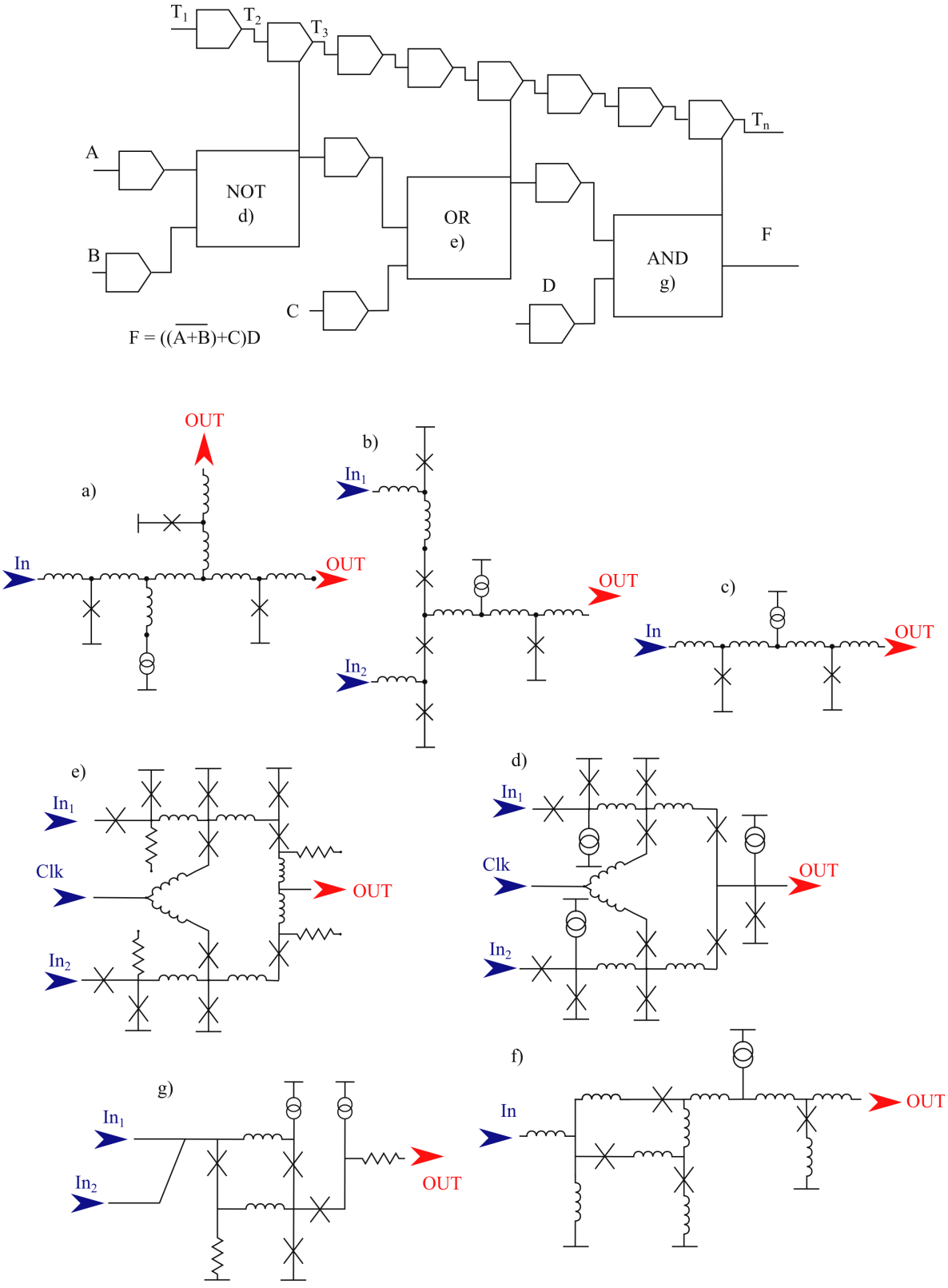


Figure 2.2: Schematic representation of RSFQ circuit suggested by Likharev, Semenov and Mukhanov [72] and different possible circuits a) Splitter, b)Merger, c)JTL, d)AND, e)OR and f)DC/SFQ. Circuits adapted from Suny/Stony Brook RSFQ cell library [20].

Materials and cell libraries; Much of the early work in RSFQ circuity was focused on the development of common cell libraries that can be used to construct complex circuitry for very fast electronics In 2002 Febvre *et al.* [73] performed a comparative study of RSFQ cell libraries based on low T_c $Nb/Al_2O_3/Nb$ tunnel junctions and high T_c $Dr_yBa_2Cu_3O_{7-\delta}$ (as the electrode material) and $PrBa_2Cu_{3-x}Ga_xO_{7-\delta}$ (as the tunnelling barrier) with an emphasis on clock frequency limits in the hope of constructing complex circuitry from a common cell library like the ones found in the Suny/Stony Brooks group [20] which can integrated into optical or microwave signal circuits.

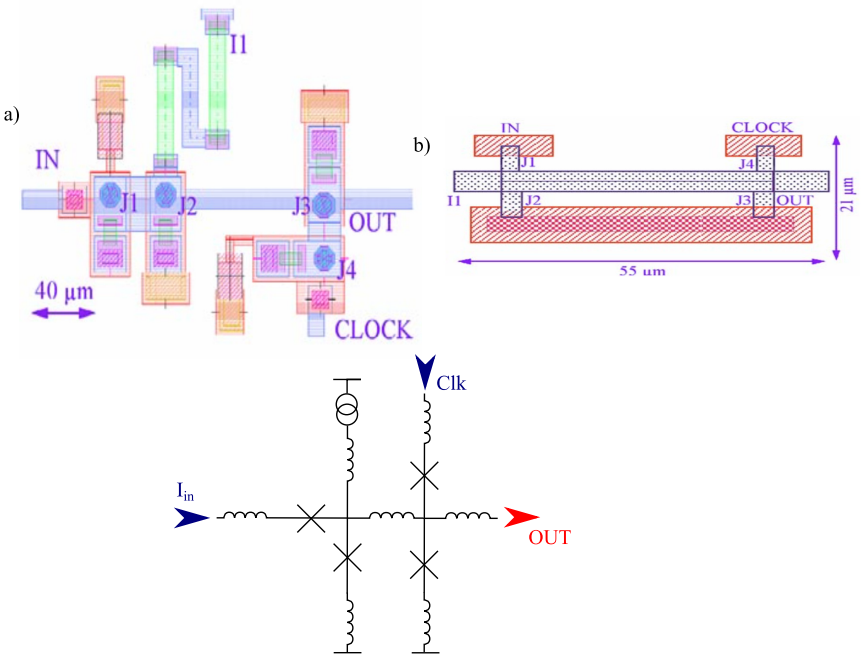


Figure 2.3: Test circuit used by Febvre *et al.* and equivalent (a) low T_c Nb/Al-Al_2O_2/Al tunnel junctions and (b) high T_c circuits composed of $D_yBa_2Cu_3O_{7-\delta}$ as the electrodes and $PrBa_2Cu_{3-x}Ga_xO_{7-\delta}$. Adapted from Febvre *et al.* [73]

The work focused on determining the upper clock frequency limit of the different circuits and thus establishing clear operating margin for devices based on different materials. Using the circuits shown in Figure 2.3 they undertook a two step process, first by optimising the devices for the maximum possible frequency to reach the

highest margin of operation[3]. The results are shown in Figure 2.4

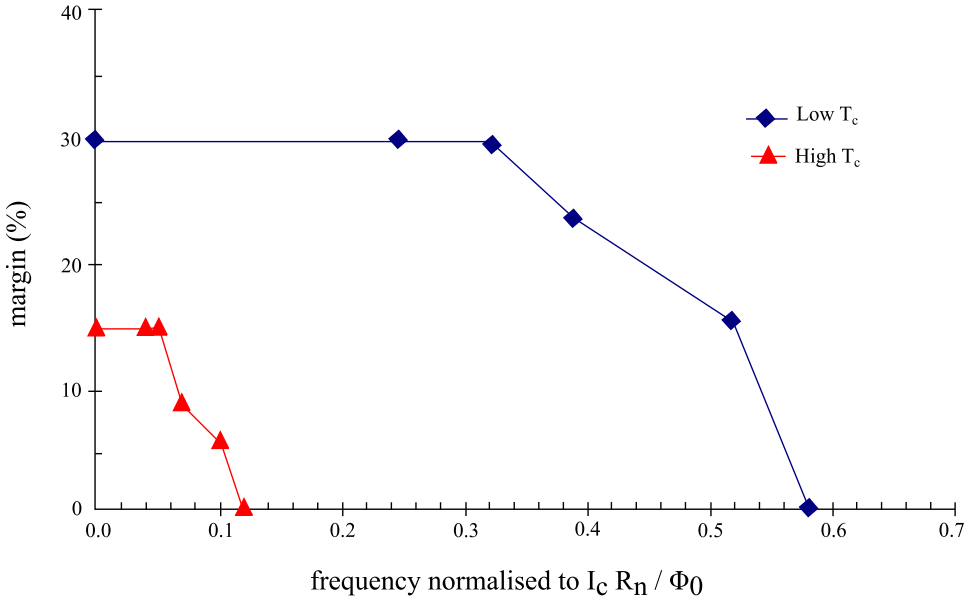


Figure 2.4: Operating margins of both low and high T_c devices. The low T_c device offers higher operating margins up to 30% compared to high T_c devices were it only stands at 15%. Adapted from Febvre *et al.* [73]

Since the establishment of very reliable cell libraries for RSFQ circuits, work has focused on the decision elements of all such devices and as such research in improving the preformance and decision making of Josephson comparator utilising low and high T_c material, below are a few examples of such efforts and a brief description of their results.

[3]the term margin of operation is used to describe the upper and lower limit at which the Josephson comparator can be operated without any loss of preformance, the larger the margin of operation the more resistant the Josephson comparator is to fluctuations in input currents and voltages allowing for easier operation.

2.2 Josephson comparator

As the only element in the RSFQ circuit family that provides logical data processing, the Josephson comparator is an important component of any fast samplers and analogue to digital convert circuits and is the determining element of their performance. Sometimes referred to as a balanced comparator, where two identical junctions (or with very similar parameters) are connected by a common bias source which is usually the processed signal, a basic setup is shown in Figure 1.26. Due to their importance work has been carried out to understand the fundamental limitations of such devices. In the following sections we review the theoretical and experimental studies into the performance of the comparators

2.2.1 Theoretical studies; comparator sensitivity, resolution and error

Theoretical models of Josephson comparators have focused on a particular set of devices, by using small inductance loop the source of the SFQ pulses can be lumped together as phase generators, whilst the grey zone is seen in terms of a probability P where the switching as mentioned in Section 1.4.3 is defined as the transition from "0" meaning no switching and "1" representing full switching and follows a Gaussian process where for a balanced comparator ΔI_{x} describes the total range of current where the transition from "0" to "1" occurs, a graphical representation of the switching is shown in Figure 2.5, whilst the switching probability is also described mathematically as:

$$\Delta I_{\mathrm{x}} = \left| \frac{\partial P}{\partial I} \right|_{I=0}^{-1} \tag{2.1}$$

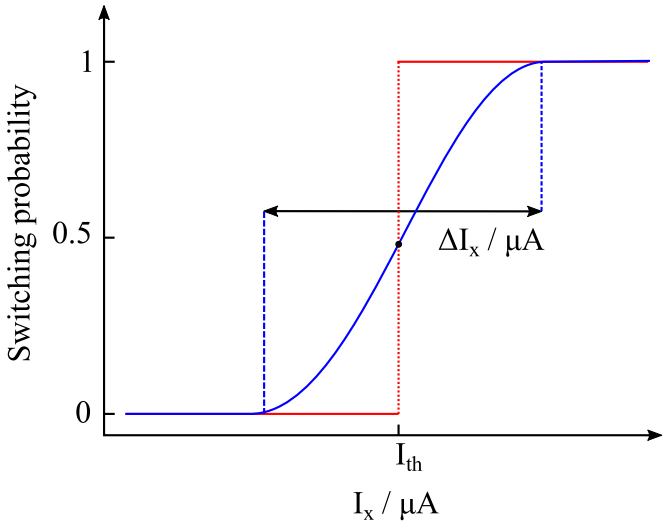


Figure 2.5: Graphical representation of the switching probability. The red line represents an ideal Heaviside vertical step describing a zero or infinitely small grey zone, whilst the blue line represents the scenario in a real device where thermal and other noise sources result in a smoothing of the Heaviside function, ΔI_{x} describes the range of currents at which the transition from "0" to "1" switching probability occurs at. I_{th} represents the current value at which the switching probability stands at 0.5, if the comparator is described as a balanced comparator then $I_{\mathrm{th}} = 0\mu A$.

Sensitivity and Resolution: In 1991 based on experimental observations, Filippov and Korne [74] proposed a numerical model that predicts the effect of thermal fluctuations on the grey zone width of a simple Josephson comparator, as such defining fundamental limits effecting the sensitivity of a balanced comparator. By using the phase generator lumped circuit definition, Filippov and Kornev fabricated and tested the circuit shown in Figure 2.6.

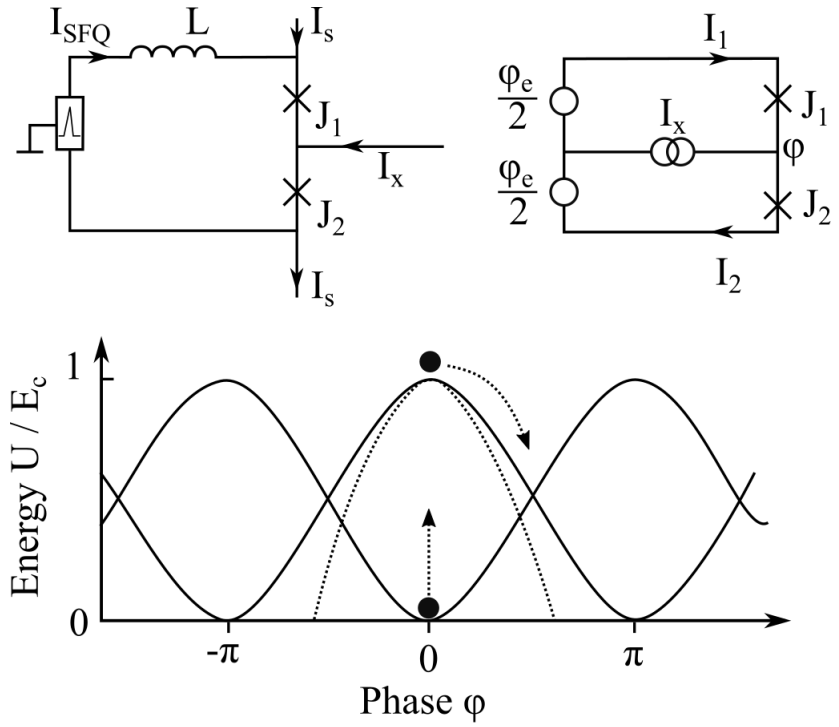


Figure 2.6: Schematic representation of the experimental (top left) and equivalent circuit (top right) used by Filippov and Kornev. The energy potential diagram of the phase φ (bottom) is calculated as a functions of the phase difference of the two comparator junctions $\varphi = \varphi_1 - \varphi_2$. Whilst φ_e is the incoming phase from the preceding circuit. Adapted from Filippov and Kornev [74].

Using the RSCJ model and the washboard analogy, the phase difference φ is described as:

$$m\ddot{\varphi} + 2m\gamma\dot{\varphi} + m\omega^2(t)\sin(\varphi) = F + F_{\mathrm{f}} \tag{2.2}$$

where

$$m = 2C_{\mathrm{J}}\left(\frac{\hbar}{2e}\right)^2, \qquad \gamma = (2R_{\mathrm{N}}C_{\mathrm{J}})^{-1}, \qquad \omega^2(t) = \left(\frac{2e}{\hbar C_{\mathrm{J}}}\right) I_{\mathrm{c}} \cos\left(\frac{\varphi_{\mathrm{e}}(t)}{2}\right)$$

$$F = -\frac{I\hbar}{2e}, \qquad F_{\mathrm{f}} = \frac{I\hbar}{2e}(I_{\mathrm{f2}} - I_{\mathrm{f1}})$$

where I_{f1} and I_{f2} are the fluctuation currents.By assuming that the inversion of the energy potential through increasing φ_{e} depends on a rate κ so that any changes in

$\varphi_{\mathrm{e}}(t)$ occurs in such a way that the frequency $\omega^2(t)$ satisfies;

$$\omega^2(t) = \left(\omega_0^2 + \omega_1^2\right) e^{-\kappa t} - \omega_1^2 \tag{2.3}$$

where $\omega_0^2 = (2eI_{\mathrm{c}}/\hbar C_{\mathrm{J}}) \cos(\varphi_{\mathrm{e}}(0)/2)$ and $\omega_1^2 = (2eI_{\mathrm{c}}/\hbar C_{\mathrm{J}}) \cos(\varphi_{\mathrm{e}}(\infty)/2)$. The initial state of the determines the movement of the phase potential and in particular the inverted system. If φ is small enough it allows for Equation 2.2 to be linearised resulting in the Langevin equation;

$$m\ddot{\varphi} + 2m\gamma\dot{\varphi} + m\omega^2(t)\varphi = F + F_{\mathrm{f}} \tag{2.4}$$

Omitting the complex derivation of the solution to Equation 2.4 which can be found here [74]. By linearising φ_{e} and taking its initial value as $\varphi_{\mathrm{e}}(0) = \arcsin(I_{\mathrm{s}}/I_{\mathrm{c}})$ and $\varphi_{\mathrm{e}}(\infty) = \varphi_{\mathrm{e}}(0) + 4\pi/(2 + L\cos(\varphi_{\mathrm{e}}(0)))$, Filippov and Kornev proposed two expression for ΔI_{x}.

Quantum limit: when $k_{\mathrm{B}}T \ll \hbar\omega_0$, for a Josephson comparator consisting of two overdamped junctions where (ω_0/γ) if $t \gg 1/\left(\left(\gamma^2 + \omega_1^2\right)^{1/2} - \gamma\right)$ and ΔI_{x} is represented as;

$$\Delta I_{\mathrm{x}}|_{\substack{T=0 \\ \gamma \gg \omega_0}} = \left(\frac{8e^2 I_{\mathrm{c}} V_{\mathrm{c}}}{\hbar}\right)^{1/2} \frac{\lambda_0\lambda_1}{\lambda_0 + \lambda_1} \ln(\Omega/\omega_0) \tag{2.5}$$

where $\lambda_0 = \cos(\varphi_{\mathrm{e}}(0)/2)$, $\lambda_1 = \cos(\varphi_{\mathrm{e}}(\infty)/2)$ and Ω is defined as a cut off frequency and is approximately equal to $\approx 50\omega_0$.

Thermal limit: In this region, where $k_{\mathrm{B}}T \gg \hbar\omega_0$, if $t \gg 1/\left(\left(\gamma^2 + \omega_1^2\right)^{1/2} - \gamma\right)$, when conditions, $\gamma \gg \omega_1$, $\kappa \ll \omega_1^2$ or $\gamma \gg \omega_1$, $\kappa \gg \omega_1/\gamma$, then the expression for ΔI_{x} becomes;

$$\Delta I_{\mathrm{x}} = (4\pi I_{\mathrm{c}} I_{\mathrm{T}})^{1/2} \left(\frac{\lambda_0\lambda_1}{\lambda_0 + \lambda_1}\right)^{1/2} \tag{2.6}$$

where

$$I_{\mathrm{T}} = \frac{2ek_{\mathrm{B}}T}{\hbar} = \frac{2\pi k_{\mathrm{B}}T}{\Phi_0}$$

Employing the circuit shown in Figure 2.6 Filippov investigated the effect of temperature, clock frequency and SFQ pulse duration on the size of the grey zone. using the assumptions that the clock frequency rate is slower than the Josephson plasma frequency $\omega_{\mathrm{p}} = \sqrt{2\pi I_{\mathrm{c}}/\Phi_0 C}$, Filippov looked in to the effect of temperature on the grey zone ΔI_{x} and comparing the results to those from the model introduced earlier. Results are shown in Figure 2.7. Filippov also found that when the clock speed $d\varphi_{\mathrm{e}}/dt$ decreases results in the grey zone ΔI_{x} shrinking [75].

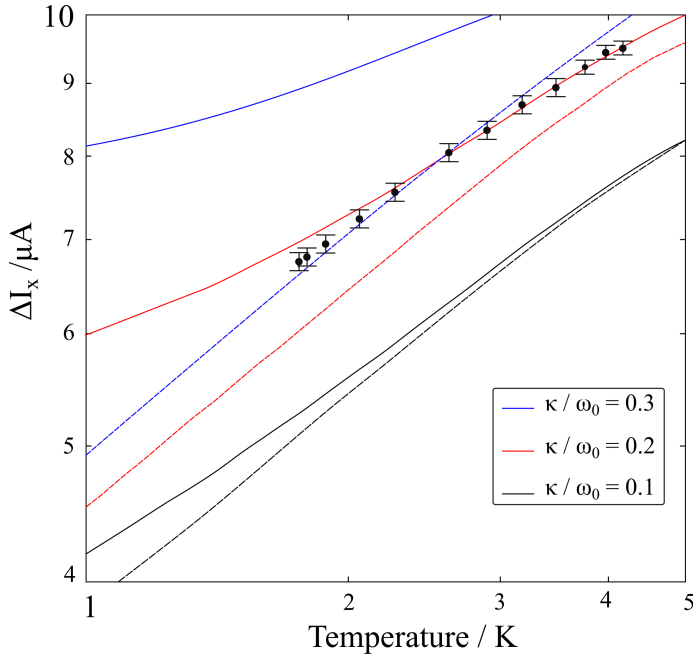


Figure 2.7: Temperature dependence of the grey zone at different ratios of κ/ω_0 marked as black circles with error bars present. The solid lines represent the grey zone derived from first principles according to equations present in Filippov [74] whilst the dashed lines represent the pure thermal model according to Equation 2.6. There is good correlation between the first principle model and the data up to 2 K at which point the purely thermal model becomes a better fit. Adapted from Filippov *et al.* [75]

Errors: The low switching energy of RSFQ circuits whilst very desirable does mean that when operated in the thermal region the probability of thermally induced switching, a process known as false switching can occur, this results in false readouts and is highly undesirable. Due to the use RSFQ circuitry as large scale high speed digital signal processor understanding and controlling error rate becomes very important. Theoretical and experimental work has been done by Herr *et al.* [76–78] and Ortlepp *et al.* [79, 80] towards the developments of modules that quantify errors in such circuits.

$$x_i^{'} = f_i\left(\underline{x}, \underline{u}, \tau\right) + \Gamma_i\left(\tau\right) \qquad i = 1...k \tag{2.7}$$

$$\frac{\partial W}{\partial \tau} = \left\{ -\sum_i \frac{\partial}{\partial x_i} f_i\left(\underline{x}, \underline{u}, \tau\right) + \sum_i \frac{\sigma_i}{2} \frac{\partial^2}{\partial x_i^2} f_i\left(\underline{x}, \underline{u}, \tau\right) \right\} W \tag{2.8}$$

Using the Fokker-Planck Equation 2.8 constructed from a set of stochastic Equations 2.7 which represent the Josephson comparator system both Herr and Ortlepp *et al.* developed a set of equations that model the rate of error in a superconducting circuit. Beginning with the work done by Herr *et al.*. Focused on dynamic error which arises from transfer of SFQ pulses across an RSFQ circuit. Using a slow 10 GHz clock frequency they developed an error detection circuit as shown in Figure 2.9 using HYPRES 1 kA/cm^2 Nb tunnel process [19].

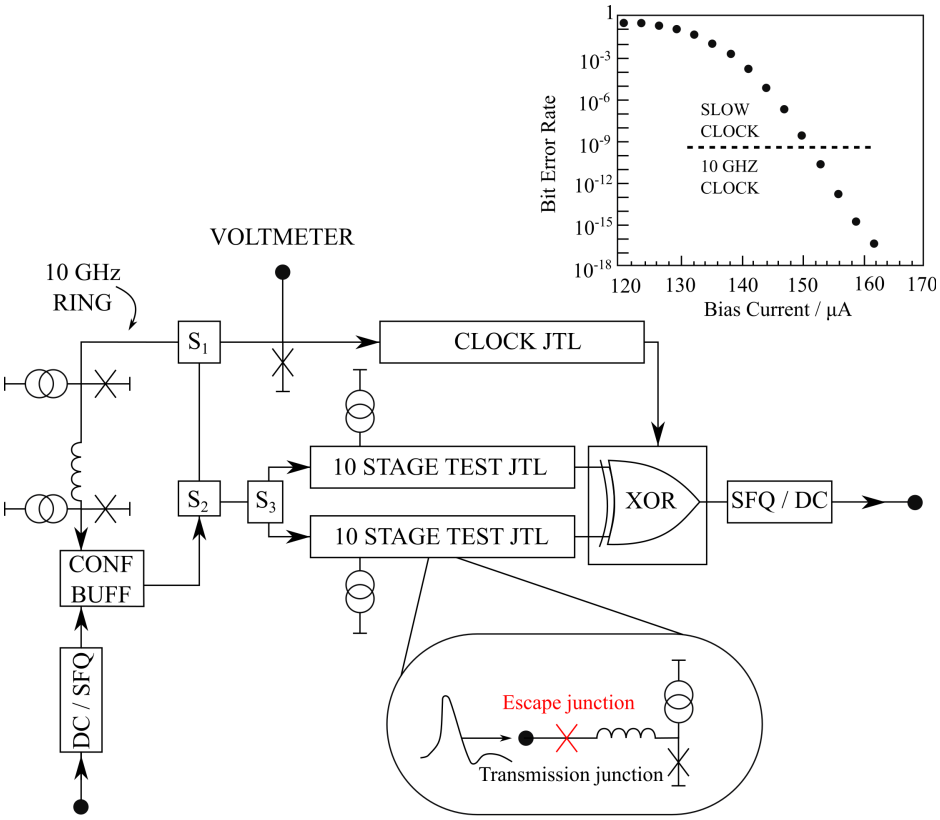


Figure 2.8: Set-up of Herr *et al.* error rate experiment. The inset demonstrates an SFQ pulse reaching the two junctions that make the Josephson comparator of the JTL stage and the measured error rate. Adapted from Herr and Feldman [77].

The DC/SFQ generates an SFQ pulse that travels to JTL via the buffer where it circulates at a frequency of 10 GHz, changing the biasing of escape junctions results in the SFQ pulse exiting the the ring. whilst the pulse is circulating an SFQ pulse splitter labelled "S_1" directs a pulse towards the clock JTL whilst splitters S_2 and S_3 direct the SFQ pulse towards 2 identical 10 stage JTL circuits (which have an escape junction as shown in Figure 2.8) which in turn transfers a pulse which triggers the XOR circuit. Correct operation comes from both JTL circuit stages transferring pulses to the RSFQ XOR circuit which in turn results in zero output. In the presence of error the SFQ pulse exits through an escape junctions and is detected by the SFQ/DC stage and the RSFQ XOR outputs a logical 1. By adjusting the biasing current of the 2 JTL stages the frequency of errors can be

varied, from optimal bias where no SFQ pulse exit via the escape junction to where all SFQ pulses exit indicating error. Plotting the bit error rate versus the biasing current resulted in a smooth curve as shown in Figure 2.9

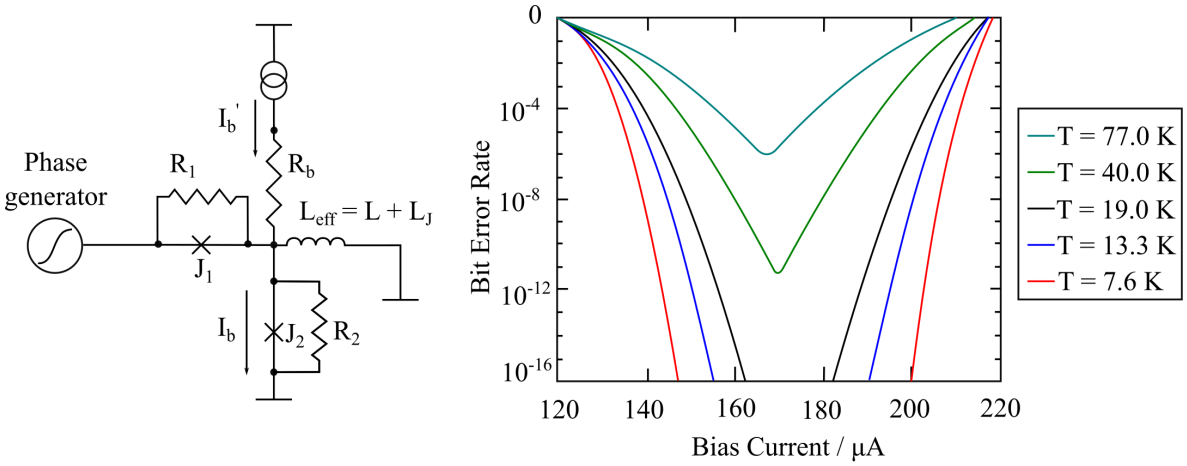


Figure 2.9: Schematic of simplified RSFQ circuit. The stages proceeding the comparator are lumped together as a phase generator. Adapted from Herr and Feldman [77].

Based on these results the group developed a theoretical model using the phase generator argument [74]. Linearisation of the phase from the phase generator which is similar to the method introduced by Filippov *et al.* but use a different approximations for their system where the phase of the phase generator is a step function described by;

$$\varphi\left(t\right) = \varphi_0 + \frac{2\pi}{1 + \exp\left(-\pi t/\tau\right)} \tag{2.9}$$

where φ_0 is the initial phase resulting from input currents of the DC/SFQ and τ is the rise time of the phase. By simplifying the circuit and representing all other components except the comparator junctions as a phase generator as shown in Figure 2.9, the switching probability of the escape junctions is modelled as an error function shown in Equations 2.10

$$\sqrt{\frac{\alpha/T}{4\pi}} \int_{I_x}^{\infty} e^{-(\alpha/T)z^2} dz \xrightarrow{I_x\ Large} \frac{1}{\pi\sqrt{\alpha/T}I_x} e^{-(\alpha/T)I_x^2} \tag{2.10}$$

Where I_{x} is current, for an asymmetric comparator as the one fabricated by Herr *et al.* is calculated as $I_{\mathrm{x}} = I_{\mathrm{b}} - I_{\mathrm{o}}$ where I_{o} is an offset current which can be used to achieve balance, T is temperature and α is a constant which depends on circuit parameters which is determined as a linear fit from the experimental bit error rate. Plotting Equation 2.10 results in the graph seen in Figure 2.9 where the minimum error rate is achieved at the balance point where $I_{\mathrm{x}} = 0$.

In order to fully understand thermal switching events the switching probability of the comparator junctions must be modelled. Using the washboard analogy Herr *et al.* introduces the parameters m, d and k as

$$m = \left(\frac{\hbar}{2e}\right) C \qquad d = \left(\frac{\hbar}{2e}\right) \frac{1}{R} \qquad \kappa = \left(\frac{\hbar}{2e}\right) \frac{1}{L_{\mathrm{eff}}} \tag{2.11}$$

the phase of the transmission junction is defined as an independent spatial variable x resulting in the phase of the escape junction equaling $\varphi(t) - x$. Constructing a Langevin equation of motion for the circuit gives;

$$\dot{x} = v \qquad \dot{v} = D_v(x, v, t) + \Gamma(t) \tag{2.12}$$

where

$$D_v(x, v, t) = \frac{-I_{\mathrm{b}}^{'} + I_{\mathrm{c1}} \sin(\varphi - x) - I_{\mathrm{c2}} \sin(x - \kappa x) + m_1 \ddot{\varphi} + d_1 \dot{\varphi} - (d_1 + d_2) v}{m_1 + m_2} \tag{2.13}$$

and the noise current in the resistor results in the stochastic force $\Gamma(t)$ with mean zero and variance;

$$D_{vv} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_b}\right) \frac{2k_{\mathrm{B}}T}{m_1 + m_2} \tag{2.14}$$

Combining all the variables to calculate the switching probability as shown in

Equation 2.8 results in the Fokker Planck equation

$$\frac{\partial W}{\partial t} = \left(-v\frac{\partial}{\partial x} - \frac{\partial}{\partial v} D_v\left(x, v, t\right) + \frac{1}{2}\frac{\partial^2}{\partial v^2} D_{vv} \right) W \tag{2.15}$$

Taking the spatial terms separately, a method known as operator splitting, the two-step Lax-Wendroff method is used to solve for the the first order partial derivative and the Crank-Nicolson method is used for the v derivative, this is known as operator splitting a computational exhaustive method due to the large grid points Solving Equation 2.15 allows the tracking of the phase of the comparator junctions;

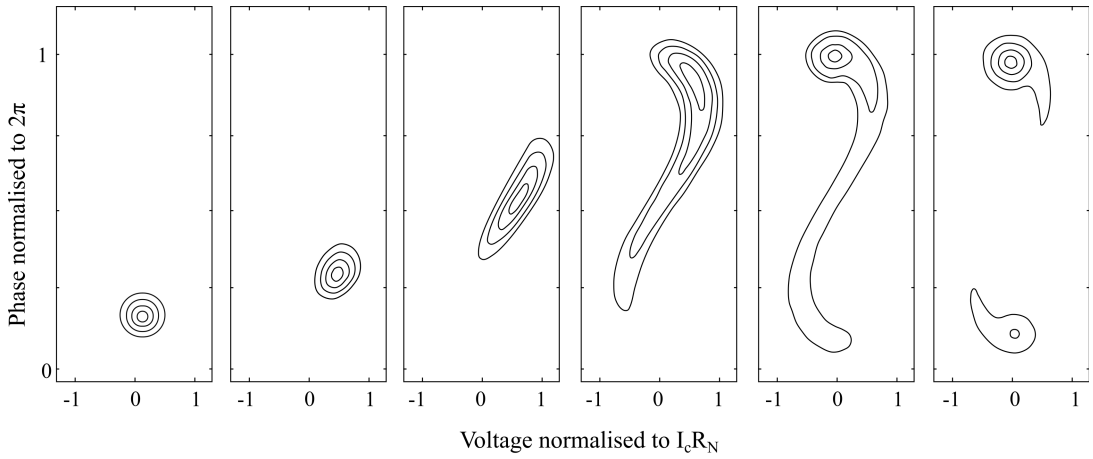


Figure 2.10: Example of time evolution of the phases probability distribution function at 3 ps apart, each frame represents probabilities of 0.47, 0.91, 0.995 and 0.9999

This method restricts modelling of switching probability to only the comparator junctions i.e. escape and transmission junctions. In 2003 Ortlepp *et al* [79]. suggested an approach that divides the RSFQ circuits into its component parts which are then characterised in terms of their switching probability. The data for the separate sections are then combined resulting in an overall switching error for the whole comparator circuit, allowing the switching probability to be tracked throughout the device, giving a more complete picture of the error which arises in an RSFQ circuit and as such does not require the complicated setup used by Herr *et al.* to track the error. Using a modification of the RSCJ equations they define

two parallel junctions like those in a JTL (see Section 1.4.3)each having its own biasing source connected to a phase generator φ as:

$$\begin{aligned}\frac{\Phi_0}{2\pi R_{\mathrm{N1}}}\dot{x_1} &= I_{\mathrm{b1}} - I_{\mathrm{c1}}\sin(x_1) + \frac{\Phi_0}{2\pi}\left(\frac{\varphi - x_1}{L_1} + \frac{x_2 - x_1}{L_2}\right)\\ \frac{\Phi_0}{2\pi R_{\mathrm{N2}}}\dot{x_2} &= I_{\mathrm{b2}} - I_{\mathrm{c2}}\sin(x_2) + \frac{\Phi_0}{2\pi}\left(\frac{x_1 - x_2}{L_2}\right)\end{aligned} \tag{2.16}$$

The Fokker-Planck equation for the circuit is then given as:

$$\begin{aligned}\frac{\partial W}{\partial t} &= W\left(2\pi\frac{R_{\mathrm{N1}}I_{\mathrm{b1}} + R_{\mathrm{N2}}I_{\mathrm{b2}}}{\Phi_0} + \frac{R_{\mathrm{N1}}}{L_1} + \frac{R_{\mathrm{N1}} + R_{\mathrm{N2}}}{L_2}\right)\\ &- \frac{\partial W}{\partial x_1}R_{\mathrm{N1}}\left(2\pi\frac{I_{\mathrm{b1}} - I_{\mathrm{c1}}\sin(x_1)}{\Phi_0}\frac{\varphi - x_1}{L_1} + \frac{x_2 - x_1}{L_2}\right)\\ &- \frac{\partial W}{\partial x_2} = \left(2\pi\frac{I_{\mathrm{b2}} - I_{\mathrm{c2}}\sin(x_2)}{\Phi_0} + \frac{x_1 - x_2}{L_2}\right)\\ &+ \frac{1}{4}\frac{4\pi k_{\mathrm{B}}T}{\Phi_0}\left(R_{\mathrm{N1}}^2\frac{\partial^2 W}{\partial x_1^2} + R_{\mathrm{N2}}^2\frac{\partial^2 W}{\partial x_1^2}\right)\end{aligned} \tag{2.17}$$

By solving Equation 2.17 analytically [81] and by ensuring that the phase of the junctions proceeding the phase generator is directly following it, this leads to three different errors [82, 83] being extracted from the solution, the first is known as a static error and is given as:

$$p_s(t) = \frac{d}{dt}\iint\limits_{x_2>\pi+\varphi} W(x_1, x_2, t)\ , dx_2\ , dx_1 \tag{2.18}$$

and the other are referred to as dynamical error and given as:

$$p_{d1}(t) = \frac{d}{dt}\iint\limits_{x_2>\pi} W(x_1, x_2, t)\ , dx_2\ , dx_1 \tag{2.19}$$

$$p_{d2}(t) = \frac{d}{dt}\iint\limits_{x_2>3\pi} W(x_1, x_2, t)\ , dx_2\ , dx_1 \tag{2.20}$$

Using Equations 2.18-2.20 it is possible to track errors in circuit as a function of time as shown in Figure 2.11.

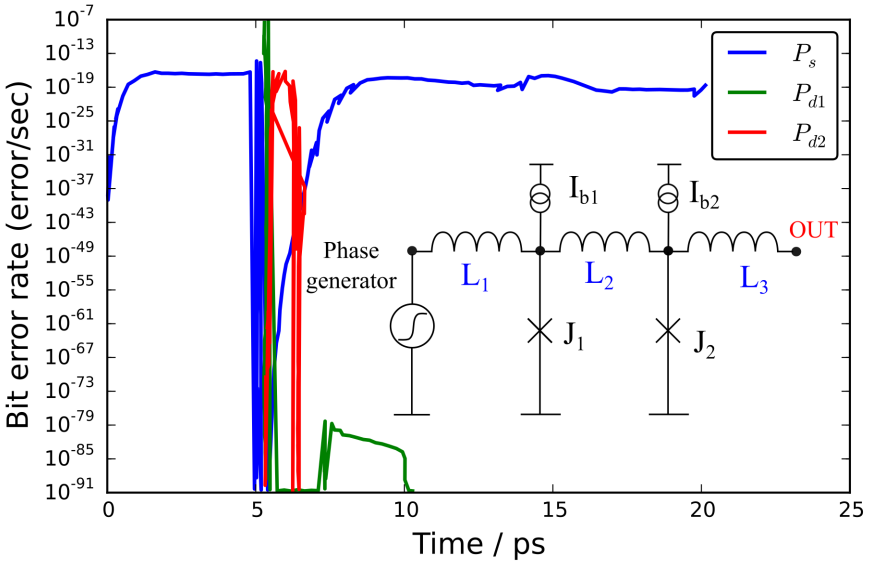


Figure 2.11: All three error rates and the corresponding circuit. Static error seem to be the biggest contributor to overall error in the circuit, as the phase generator is turned on at $t = 5$ ps, there is a period of a few picoseconds where the most likely due to circuit transient the dynamic error has a bigger contribution to overall error until the circuit settles where static error then begins to dominate again. Adapted from Ortlep *et al.* [79]

However this method is restricted to phase generator type circuits with low clock frequency similar to the those introduced by Filippov *et al.* [74]. In addition to the work mentioned so far into the error rate of RSFQ circuits work has also be done by Goldobin *et al.* [84] and Polonsky *et al.* [85], where a circulating SFQ pulse was observed not to decay for several hours suggesting a BER of $< 10^{-14}$.

2.2.2 Experimental studies; Low T_c devices

In almost all cases, the material of choice for low temperature Josephson comparator is niobium Nb, due to its high critical temperature when compared with other low T_c materials meaning it can with stand large magnetic fields and is easily deposited using sputtering techniques. The basic set-up of any RSFQ Josephson comparator is described in Figure 1.26.

Design guidelines: In 2010 Thomas Ortlepp *et al.* [86] tested through simulations and experimental observations. Using 3 circuits shown in Figure 2.12 as base and altering different parameters 8 different Josephson comparator circuits are realised. The changes are detailed in Table 2.1.

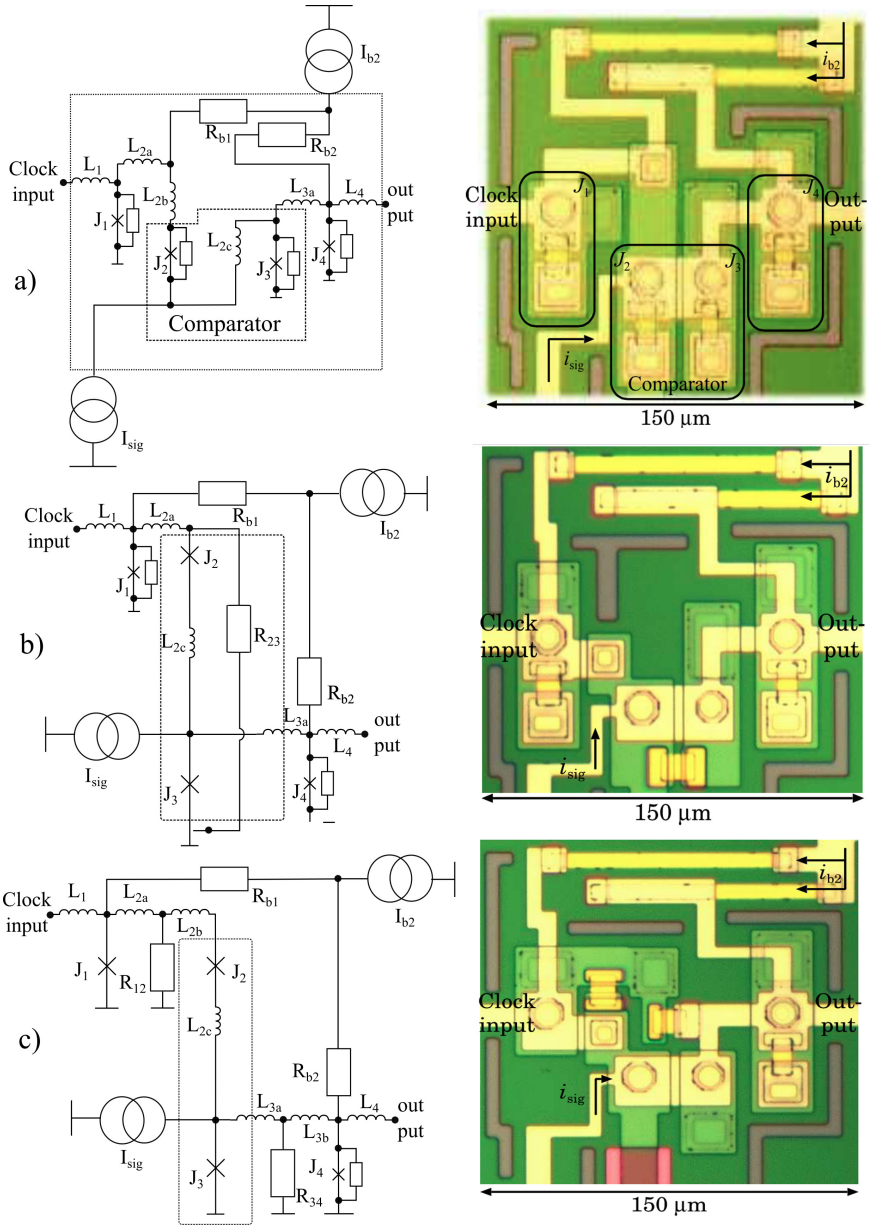


Figure 2.12: Circuit and optical images of the basic layout of all the comparators tested by Ortlepp *et al.* All devices fabricated from low T_c $Nb/Al_2O_3/Nb$ tunnel junctions. Adapted from Bjoern and Ortlepp [86].

Using comparator 2.12 as a reference device all other circuits were modified with respect to one topological or design parameter aspect. Ortlepp *et al.* investigated the effect of critical current of the junction J_2 on comparators 1-a, 1-b and 1-c, comparators 1-a. and 1-c are identical except for the inductors that make up the loop L_{2a} and L_{2b} whilst comparator 3 is obtained by removing the shunt resistor from comparator 1-a. Comparators 2-a, -b, -c and -d utilise the presence of a shared biasing source at I_{b2} which is directly connected to the driver junctions J_1, in addition to this comparators 2-b and -c share a common shunt resistor R_{23}. Common damping resistors $R_{12}$and R_{34} are included in the centre of the comparator loop made up of J_1 - J_2 - J_3 and the output loop consisting of $J_3 - J_4$ in comp2-d, resulting in a low pass filter for the noise current of the resistors forming due to the loop indcantce and the damping resistor. All of these modifications are summarised in Table 2.1.

Name	1-a	1-b	1-c	2-a	2-b	2-c	2-d	3
Figure	2.12a	2.12a	2.12a	2.12a	2.12b	2.12b	2.12c	2.12a
$I_{c1}\,(\mu A)$	250	250	250	250	250	250	250	250
$I_{c2}\,(\mu A)$	200	175	225	200	200	200	200	200
$I_{c3}\,(\mu A)$	150	150	150	150	150	150	150	150
$I_{c4}\,(\mu A)$	200	200	200	200	200	200	200	200
β_{c1}	1	1	1	1	1	1	$\gg 1$	1
β_{c2}	1	1	1	1	$\gg 1$	$\gg 1$	$\gg 1$	$\gg 1$
β_{c3}	1	1	1	1	$\gg 1$	$\gg 1$	$\gg 1$	$\gg 1$
β_{c4}	1	1	1	1	1	1	1	1
$R_{xx}\,(\omega)$	-	-	-	-	0.75	3	0.75	-
L_1 (pH)	2.1	2.1	2.1	2.1	2.2	2.2	2.2	2.1
L_{2a} (pH)	3.4	3.4	3.4	2.2	1.9	1.9	1.0	3.4
L_{2b} (pH)	1.0	1.0	1.0	0.3	-	-	1.0	1.0
L_{2c} (pH)	1.3	1.3	1.3	1.3	1.5	1.5	1.3	1.3
L_{3a} (pH)	3.8	3.8	3.8	3.8	3.8	3.8	2.1	3.8
L_{3b} (pH)	-	-	-	-	-	-	2.1	-
L_4 (pH)	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2

Table 2.1: Design parameters of Josephson comparator where $R_{b1} = R_{b2}$ and R_{xx} is the damping resistors R_{12}, R_{23}, R_{34}, The values $\beta_c \gg 1$ implies an unshunted junction. Adapted from Bjoern and Ortlepp [86].

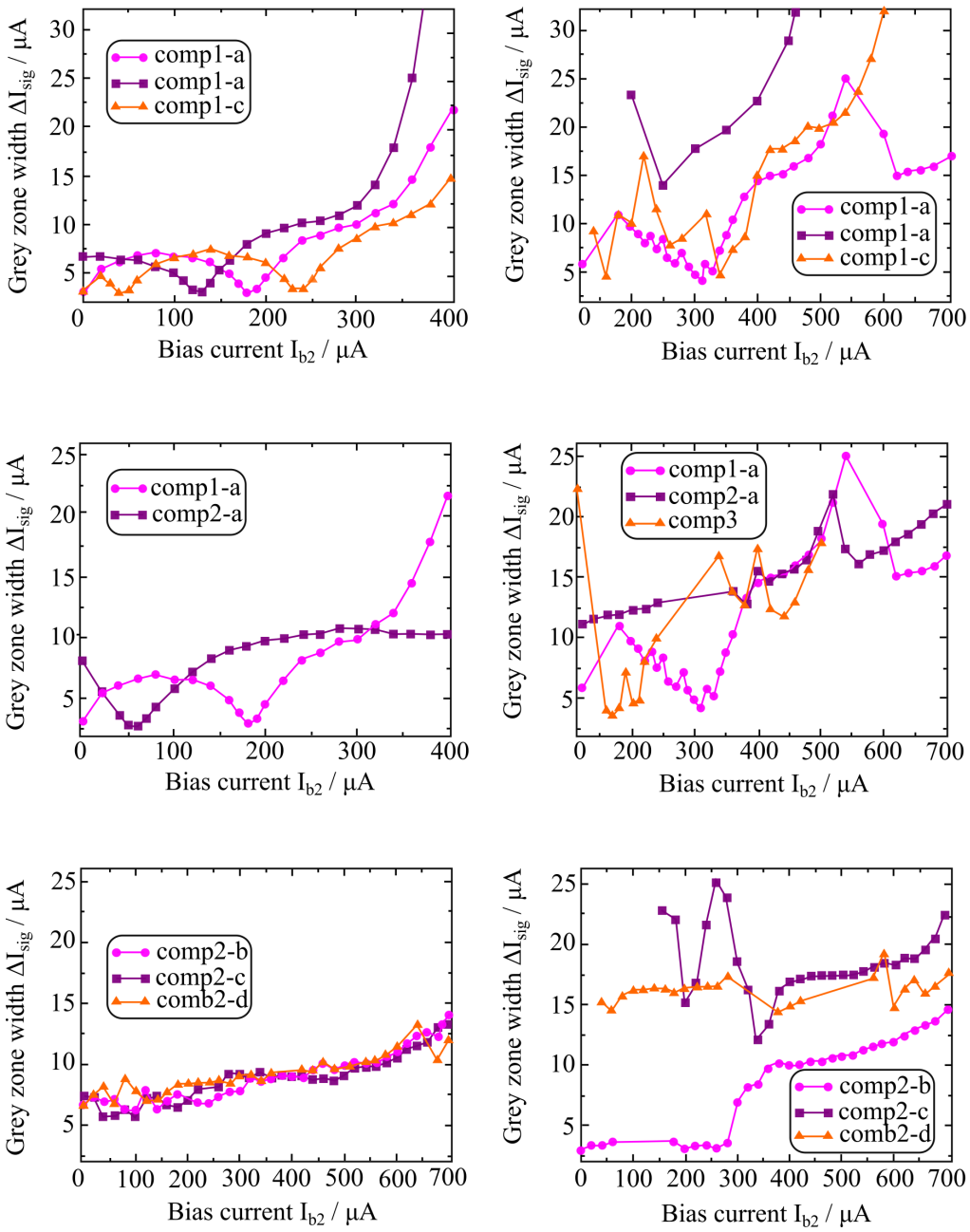


Figure 2.13: The left column are JSIM simulation results whereas the right column show measurement results. Adapted from Bjoern and Ortlepp [86].

The results obtained from both simulations and experimental testing is summarised in Figure 2.13. As of 2010, Bjoern and Ortlepp reported a grey zone width of 3.2 μA lower right graph of Figure 2.13, one of the smallest recorded at 4.2 K using comparator 2-b which has the small common shunt resistor. They attribute

this to their ability to separately fine tune the biasing current of the comparator cell. In addition to the smallest grey zone Bjoern and Ortlepp suggest the following guide lines for reducing the size of the grey zone;

- The addition small common shunt resistors such as R_{23} for comparator junctions
- Direct bias source connections to driver and output junctions
- A large non-storing total comparator loop inductance

Optimisations (speed and accuracy): Ortlepp *et al.* [87] have also looked into improving the accuracy and speed of Josephson comparator again in terms of grey zone width. Using the circuit describes in Figure 2.14 the trade-off between speed and accuracy was investigated via simulation and analysis of comparator switching times.

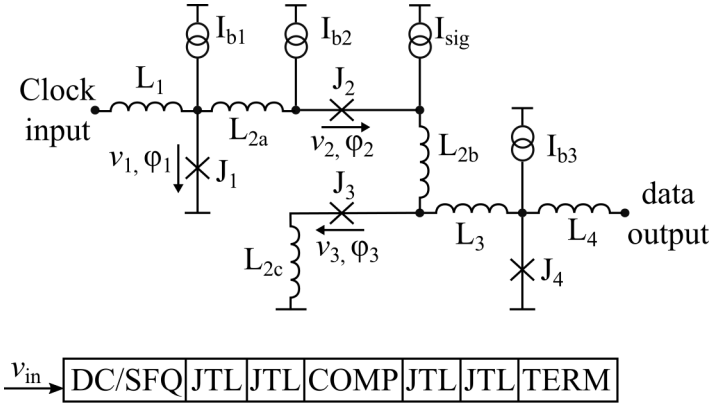


Figure 2.14: Circuit digram of comparator and block diagram whole device used in simulations, the block labelled TERM represents a 0.7 Ω termination resistor. Adapted Bjoern and Ortlepp [87].

This was carried out by altering biasing currents, total inductance of comparator and output loops, β_c, operating temperature, Junction critical currents and current density. A short summary of the influence of the six parameters on the comparator performance is given in Table 2.2.

Parameter	Modification	Benefit
Bias supply	Direct connection to driver and output junction	Larger bias margins
Loop inductance	High value	Accuracy
	Low value	Speed
McCumber parameter	$\beta_{c2}<1<\beta_{c3}$	Speed
Critical current density	High value	Speed and partly accuracy
Operating temperature	Low	Accuracy
	High	Speed

Table 2.2: Influence of different parameters on comparator performance. The β_c values refer to the Stewart-McCumber parameters for junctions J_2 and J_3 shown in Figure 2.14. Adapted Bjoern and Ortlepp [87].

By decreasing the operating temperature, the grey zone width can be reduced until a lower limit arising due to quantum noise. On the other hand, due to the lack of thermal energy at low temperatures, the switching time dramatically increases, especially for signal currents close to the threshold current. Consequently, the trade-off between speed and accuracy also extends to the operating temperature.

Clock frequency: In 2011 Haddad *et al.* [88] investigated the relationships between grey zone and clock frequency using the circuit is described in Figure 2.15

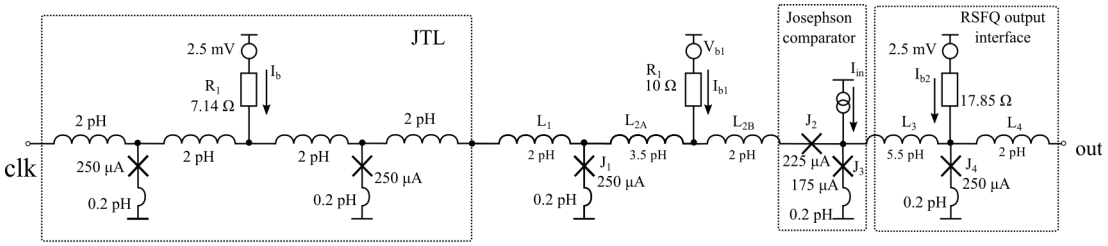


Figure 2.15: Circuit digram of Josephson comparator, a section of the Josephson Transmission Line and the RSFQ output designed by Haddad *et al.* [88].

The bias current sources are realised by voltage sources in series with on-chip resistors as assumed for the simulations. The comparator circuit is driven by a clock pulse which is transmitted to the comparator by switching of J_1. Only one of the two junctions (J_2 or J_3) is able to switch when a clock pulse triggers the comparator. The signal current I_{in} determines which one will switch. Ideally,

if $I_{in} > I_{th}$, J_3 switches otherwise J_2 switches, where the parameter I_{th} is the threshold current of the comparator. Figure 1.26 illustrates the functionality of the Josephson comparator and shows schematically the SFQ pulses, which are produced by the switching of J_1, J_2, J_3 depending on the input signal current I_{in}.

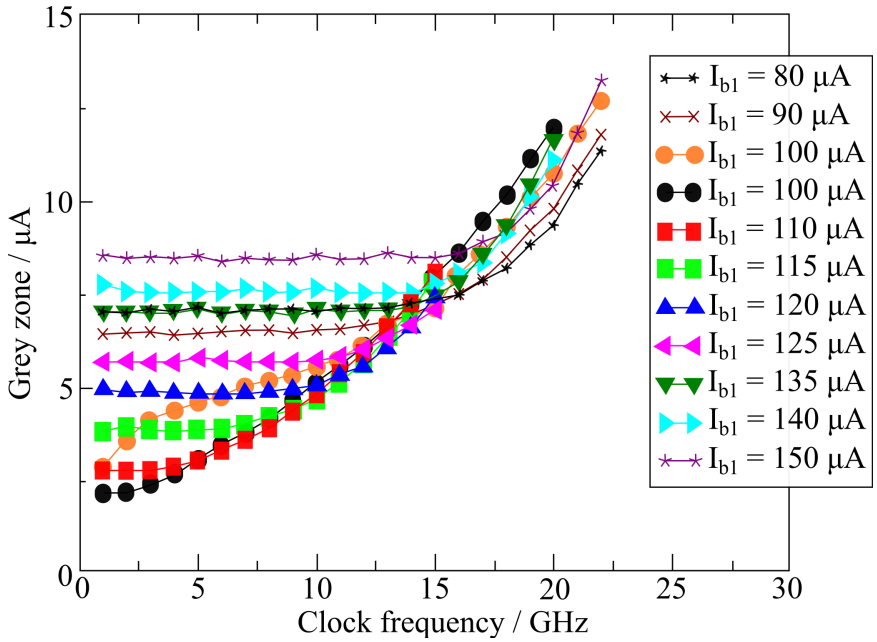


Figure 2.16: Graph showing the relationship between clock frequency and the grey zone at different biasing values of I_{b1}. At the lower I_{b1} currents the increasing the clock frequency dose not effect the grey zone it is only after a threshold frequency is reached that an increase in clock frequency translates to an increase in grey zone. Adapted Haddad *et al.* [88].

Ortlepp *et al.* found that the narrowest grey zone was achieved for a bias current 107 μA at I_{b1} when compared to the other bias sources I_b and I_{b2}. Deviation from this bias current at I_b resulted in a larger grey zone width. Ortlepp *et al.* identified a clear relation between clock frequency and grey zone. The grey zone remains constant for all clock frequencies below a characteristic frequency f_c. Above this frequency an increase of the grey zone was observed which was temperature independent. To achieve the lowest grey zone width required careful adjustment of bias currents.

I_{b1}/μA	GZ / μA	f_c / GHz
80	7.17	16
90	6.55	13
100	Not defined	Not defined
107	2.21	2
110	2.88	2
115	3.93	7
120	4.93	10
125	5.77	12
135	7.11	14
140	7.64	15
150	8.5	16

Table 2.3: Table of characteristic frequency f_c and recored grey zone.Adapted Haddad *et al.* [88].

This process is only suitable for systems with very few comparators, as used in A/D converters or sensor systems. Ortlepp *et al.* reported a clock frequency of 15 GHz, the grey zone is almost constant between 80 and 140 μA. This fact is very important for the design of comparators in digital circuits, because the bias current requires some margin to allow complex circuits to work in the presence of process variability such as the critical current spreads in fabricated device.

Low T_c ADC: As the name suggests analogue-digital converters take a continuous voltage or current (Analogue) input converting it into a N-bit digital output at a rate dictated by the sampling frequency f_s. Superconducting ADC commonly split into two categories *Nyquist sampling* and *oversampling* ADCs. One of the earliest implementations of ADC utilising RSFQ technology used the oversampling technique in a sigma-delta modulator [89]. Przbyszt *et al.* [90] tested a high speed RSFQ circuit. By utilising a large inductor (Σ) to integrate a voltage signal which is then fed to a single Josephson (Δ) junction which takes the resultant integrated current and produces SFQ pulses. The basic set-up of this sigma-delta modulator is described in Figure 2.17. The buffer stage acts as a low pass filter ensuring that the SFQ pulses do not travel back down through the circuit.

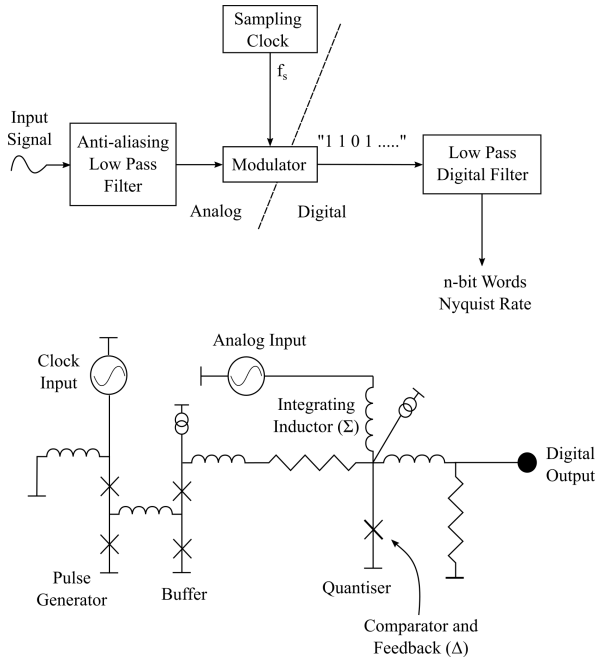


Figure 2.17: Block diagram of sigma-delta modulator ADC and schematic diagram of sigma-delta modulator fabricated by Przbyszt *et al.* using 6 kA/cm^2 $\mathrm{Nb/Al_2O_3/Nb}$ tunnel junctions. An analogue signal is fed into the modulator which outputs a digital signal at the sampling clock frequency. Adapted from Przbyszt *et al.* [90].

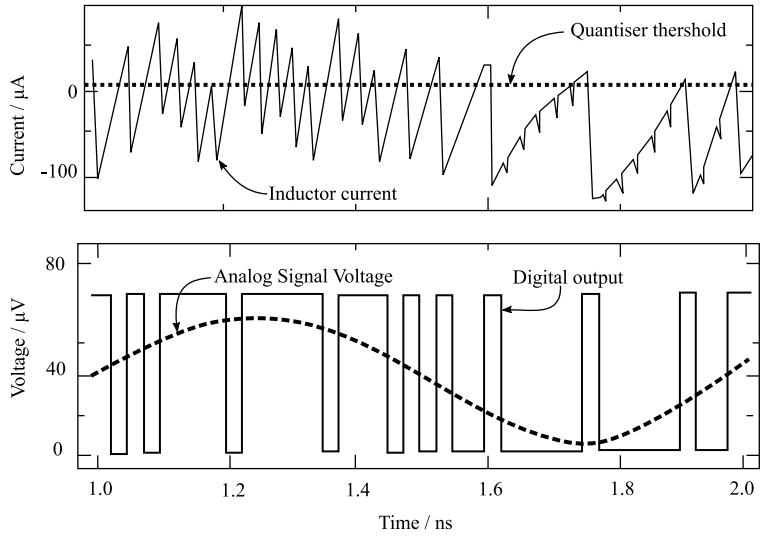


Figure 2.18: Simulations of sigma delta modulator Σ integrating inductor and 1 GHz sine wave input sampled at 40 GHz vs the digital output of for the modulator. When the current in the inductor exceeds a threshold of 7 μA results in observed current drop in the inductor during corresponding to sampling periods. Adapted from Przbyszt *et al.* [90].

2.2.3 Experimental studies; High T_c devices

The one thing most of the low temperature Josephson comparators have in common is the complexity of circuit design when the whole RSFQ circuit is taken into account. It would be preferable to have a simple comparator that is able to give fast and reliable measurements. For this reason the high T_c comparator design by Oelze *et al.* [23] is of particular interest. These circuits were fabricated on asymmetric 24° Yittria stabilised zirconia YSZ bicrystal substrates. Epitaxial, 200 nm thick YBCO films were deposited by co-evaporation and patterned by standard optical lithography with Argon ion milling. Subsequently, a 400 nm thick SiO insulation layer and a gold layer were evaporated and patterned by lift-off in order to provide the additional bias current line I_b. Figure 2.19 shows the layout of the balanced comparator consisting of a generator junction(J_g), a Josephson transmission line JTL, a buffer stage (J_1, J_2), and the comparator junctions J_3 , J_4. The equivalent circuit can be found in Figure 2.19.

The Josephson junctions had a width of $3\,\mu$m, critical currents $I_c = 340\,\mu$A, and $I_cR_n = 0.4$ mV at $T = 40$K. The inductances of the JTL were realised as holes with dimensions of $235\,\mu\text{m}^2$. These inductances were calculated using a three dimensional field analysis program 3DMLSI (see Section 4.3) and were found to be about 10 pH. The use of the additional insulator and gold layer as interconnect line, instead of a superconducting line joining the comparator loop between junctions J_2 and J_3, allowed Oelze *et al.* to decrease the inductance of the comparator loop formed by junctions J_1–J_4 down to 24 pH [23].

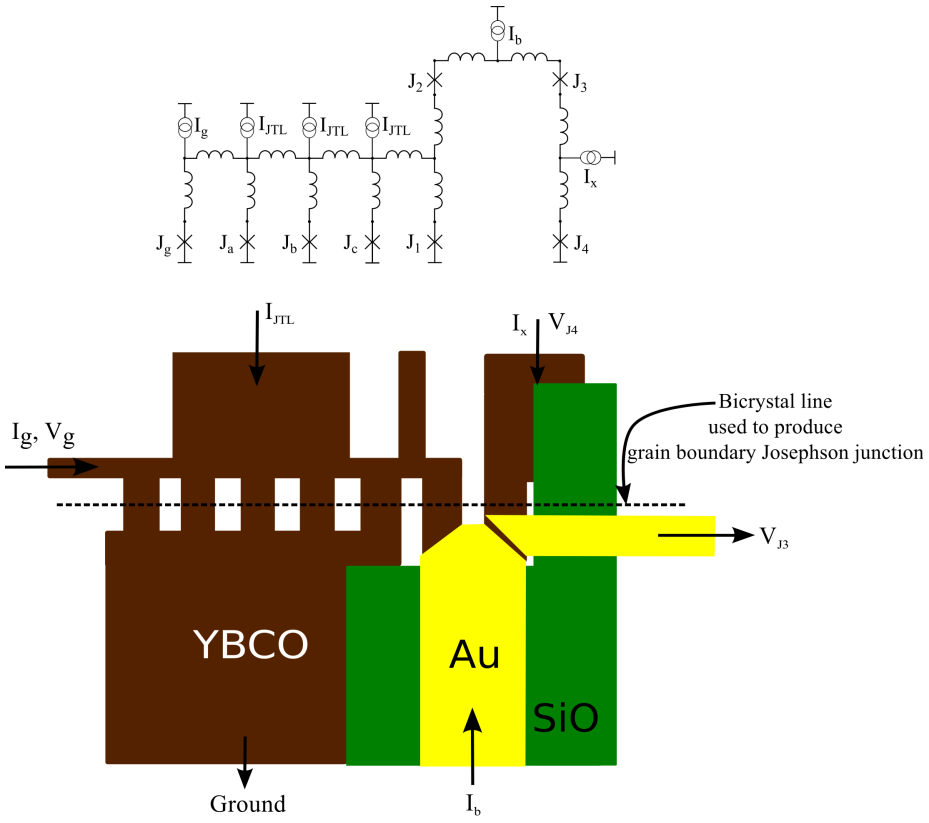


Figure 2.19: Llayout of the balanced comparator fabricated from high T_c superconductor and the equivalent circuit. Adapted from B. Oelze *et al.* [23]

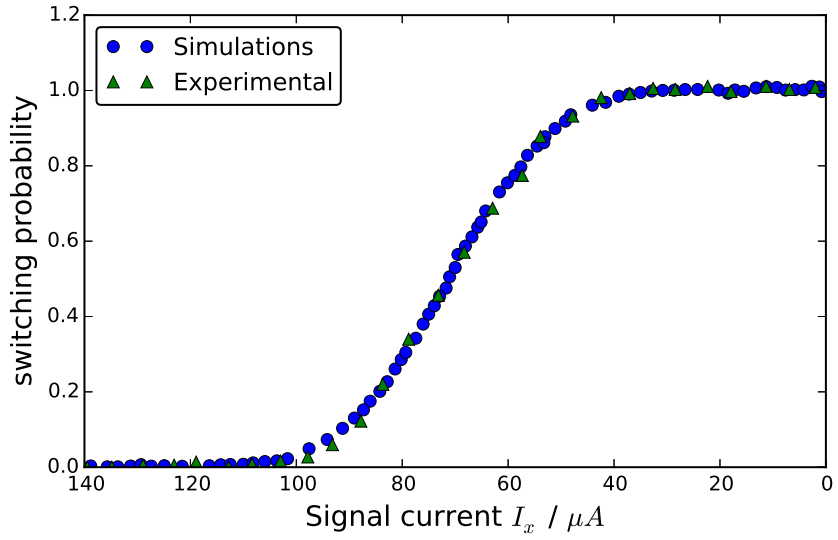


Figure 2.20: Switching probability of junction J_4 from comparator designed by Oelze et al. at $T = 40$ K. Adapted from Oelze *et al.* [23]

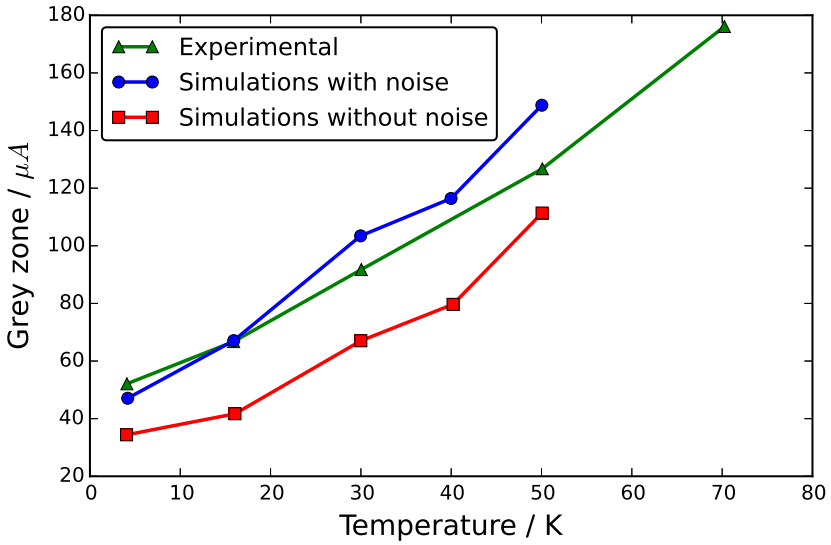


Figure 2.21: Effect of temperature on grey zone width. Generator junction voltage is maintained at $f = 95$ GHz . Adapted from Ozelc *et al.* [23]

High T_c ADC: Based on the Comparator in Figure2.19 designed and developed by Oelze *et al.* B. Ruck *et al.* [91] designed, fabricated and tested a sigma-delta modulator based on 5 μm YBCO grain boundary junctions (see dashed line in Figure 2.22) with critical current I_c of 450 μA and $I_c R_N$ product of 1 mVon a $SrTiO_3$ substrate, the resultant best grey zone measured for the comparator stood at 10 μA for a pulse frequency of 24 GHz at $T = 33$ K. Ruck *et al.* speculate that the low grey zone is in part due to the flattening of the SFQ pulses (a technique first suggested by Filippov *et al.* [75] [4]) due to the microwave losses properties of the $SrTiO_3$ substrate, with a worst case resolution of 6-bits at measurements of up to 100kHz was obtained for the sigma-delta modulator, due to restriction on measurement set-up a complete characterisation was not possible.

[4]The concept of flatting an SFQ pulse refers the the use of a smooth SFQ pulse that is spread over a longer time period normally associated with low frequency pulses Fillipove suggested that pulses should be spread over time intervals in the form $\tau = 1/f$ and the change in phase of such pulses should follow a linear behaviour where $\varphi_0(t) = 2\pi ft + constant$.

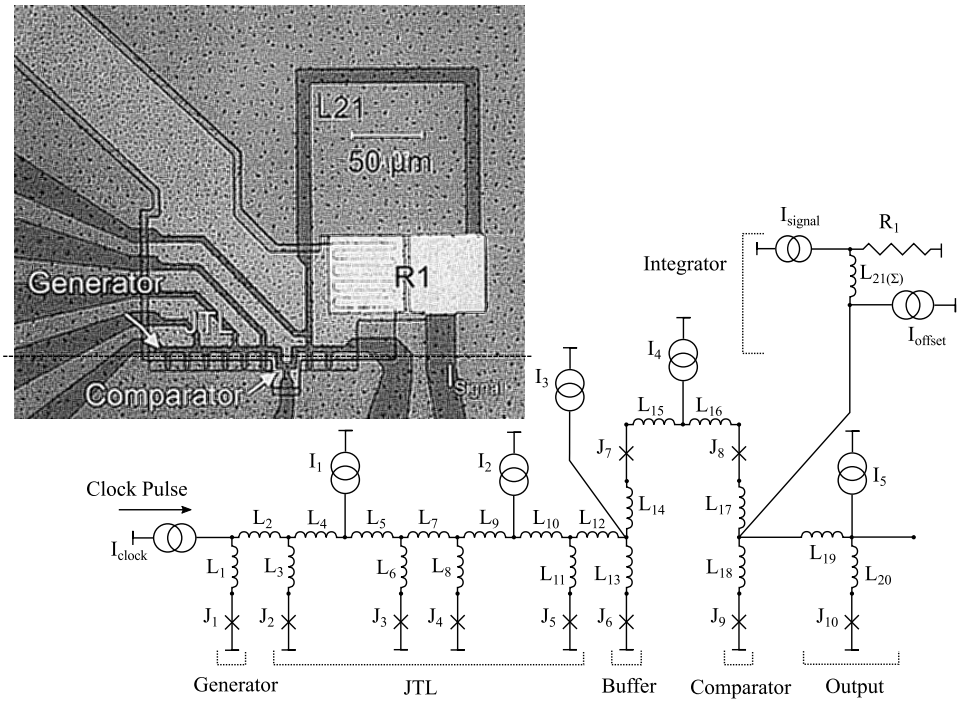


Figure 2.22: Optical image of fabricated device with the grain boundary Josephson junction marked by the dashed line and the equivalent circuit diagram. $I_{\text{clock}} = I_5 = 272\ \mu A$, $I_1 = I_2 = I_4 = 550\ \mu A$ and $I_3 = 0\ \mu A$. $L_{15} = L_{16} = 3.5$ pH and $L_{21-(\Sigma)} = 200$ pH. Adapted from B. Ruck *et al.* [91].

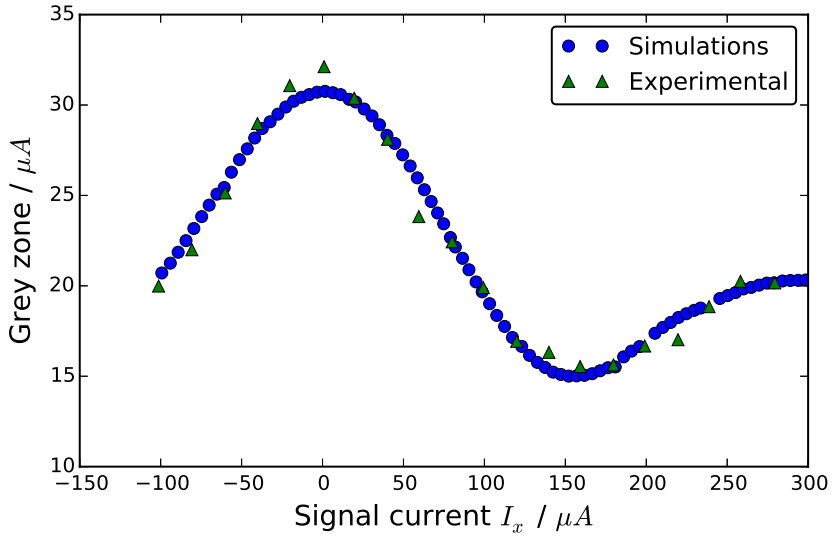


Figure 2.23: Example of Simulations and experimental observation of grey zone dependence on signal current I_{signal} when the generator J_1 junction voltage is maintained at 50 μV at $T = 68\ K$. Optimal operation of the comparator is at the minimal of the grey zone. Adapted from B. Ruck *et al.* [91].

Chapter 3

Simulation tools and fabrication techniques

3.1 JSIM

J-SIM [92] is based on JSPICE [93] a popular superconducting integrated circuit simulator previously used by Berkeley and many other organisations. JSPICE itself is based on SPICE [94] with the addition of Josephson elements. As such the JSIM has a similar input to SPICE. It utilises a fixed point method to reduce the iterations for solving the circuit related coefficient matrix at predefined time steps. Allowing the effect of noise in resistors to be modelled through the addition of stochastic voltage and current noise sources by Satchell [95] greatly enhanced the capabilities of the softwares. The basic problem solved by most circuit simulators is finding a solution to a system of simultaneous equations of the form:

$$\frac{dx}{dt} = F(x) \tag{3.1}$$

Where the solution has a second order convergence, the backwards Euler method (which is the simplest method for such problems) is ineffective. The trapezoidal

integration rule with dx/dt replaced by

$$\frac{2}{h_n}(x_n - x_{n-1}) - \left(\frac{dx}{dt}\right)_{n-1} = F(x_n) \tag{3.2}$$

where x_n is the value of x at time t_n and h_n is the nth time step, is an attractive option as it reduces the problem of solving simultaneous ordinary differential equations to solving a system of simultaneous nonlinear equations. Unfortunately no algorithm exists for directly solving nonlinear equations. Instead J-SIM employees an iterative method of which the Newton-Raphson method is a well known algorithm for solving $f(x) = 0$ [96]. The method requires an initial guess of the solution. Subsequent iteration is given by the Taylor series expansion of $f(x)$ about the previous solution, truncated to the first two terms $f\left(x^{k-1}\right) + f'(x_{k-1})\left(x^k - x^{k-1}\right) = 0$. In the case of a system of equations, the derivative is replaced by a matrix of derivatives called the Jacobian. The iterations continue until $|x^k - x^{k-1}|$ is less than some predefined number which is the convergence tolerance. Now the problem has been reduced to solving systems of simultaneous linear equations of the form

$$\frac{2}{h_n}x_n^k - J\left(x_n^{k-1}\right)x_n^k = \frac{2}{h_n}x_{n-1} + \left(\frac{dx}{dt}\right)_{n-1} + F\left(x^{k-1}\right)_{n-1} - J\left(x_n^{k-1}\right)x_n^{k-1} \tag{3.3}$$

where $J\left(x_n^{k-1}\right)$is the Jacobian of $F\left(x_n^{k-1}\right)$ evaluated at x_n^{k-1} and x_n^o is an initial guess of the solution x at time t_n. The Newton-Raphson method is second order and will converge to the solution if the initial guess x_n^o is close enough to x_n. To efficiently solve the problem J-SIM creates a matrix of a size directly proportional to the complexity of the circuit. A circuit with N nodes will have at least N equations and the matrix will be at least of dimension N by N. The LU decomposition method is well suited for these types of problems [96]. Equation 3.4 is an example

of an LU decomposition.

$$\begin{pmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} \end{pmatrix} = \begin{pmatrix} L_{11} & 0 & 0 \\ L_{21} & L_{22} & 0 \\ L_{31} & L_{32} & L_{33} \end{pmatrix} \begin{pmatrix} U_{11} & U_{12} & U_{13} \\ 0 & U_{22} & U_{23} \\ 0 & 0 & U_{33} \end{pmatrix} \tag{3.4}$$

L stands for lower triangular matrix and U stands for upper triangular matrix. Any nonsingular matrix can be decomposed to a product of two matrices where one is lower and the other is the upper triangular. Once the matrix is decomposed to LU, the solution is easily obtained in two steps. First the equation Ly = b is solved, and the solution is obtained by solving Ux = y. Both steps are simple. The former involves only forward substitutions and the later involves only backward substitutions. A more through explanation of the LU decomposition and its implementation in solving linear system of equations can be found here [96–100].

Comparison with JSPICE: Since J-SIM is based on JSPICE which itself is based on SPICE with the addition of Josephson elements. Both J-SIM and JSPICE use the modified nodal analysis method (MNA) to represent circuit equations [94]. The difference lies in the implementation of the MNA matrix and the treatment of the phase. JSPICE treats the phase of a Josephson junction as a separate voltage node to which no circuit element may be connected and the nonlinear equations are solved by Newton-Raphson method, and time integration is typically done by trapezoidal rule. A typical nodal entry of a single Josephson junction in JSPICE takes the form of:

$$\begin{pmatrix} N_+ & N_- & N_\phi \\ \frac{2C}{h_n} + \frac{1}{R} & -\frac{2C}{h_n} - \frac{1}{R} & I_c cos\phi_n^o \\ -\frac{2C}{h_n} - \frac{1}{R} & \frac{2C}{h_n} + \frac{1}{R} & -I_c \cos\phi_n^o \\ -\frac{h_n}{2}\frac{2e}{h} & -\frac{h_n}{2}\frac{2e}{h} & 1 \end{pmatrix} = \begin{pmatrix} RHS \\ I_s \\ -I_s \\ \phi_{n-1} + \frac{h_n}{2}\frac{2e}{h} v_{n-1} \end{pmatrix} \tag{3.5}$$

where

$$I_s = \frac{2C}{h_n} v_{n-1} + C\dot{v}_{n-1} - I_c \sin \phi_n^o + I_c \phi_n^o \cos \phi_n^o \tag{3.6}$$

and C, R, and I_c are junction capacitance, voltage-dependent resistance and critical current, respectively and ϕ_n^o is the guessed solution for the Newton-Raphson iterations. A major disadvantage in JSPICE when solving problems in the giga-tera hertz region for Josephson junctions revolves around the time step integration, for such oscillations JSPICE recommends the user set a maximum internal integration time step to about 0.2 ps. This time step limitation is quite fundamental as it means no time step larger than the Nyquist period can be taken. As such, the development of J-SIM focused on saving computation time instead of saving on the number of time steps. The typical MNA matrix for a Josephson junction in J-SIM takes the form of:

$$\begin{pmatrix} N_+ & N_- & N_\phi \\ \frac{2C}{h_n} + \frac{1}{R} & -\frac{2C}{h_n} - \frac{1}{R} & 0 \\ -\frac{2C}{h_n} - \frac{1}{R} & \frac{2C}{h_n} + \frac{1}{R} & 0 \\ -\frac{h_n}{2}\frac{2e}{h} & -\frac{h_n}{2}\frac{2e}{h} & 1 \end{pmatrix} = \begin{pmatrix} RHS \\ I_s \\ -I_s \\ \Phi_{n-1} + \frac{h_n}{2}\frac{2e}{h}\dot{v}_{n-1} \end{pmatrix} \tag{3.7}$$

where:

$$I_s = -I_c \sin(\phi_n^o) + \frac{2C}{h_n} v_{n-1} + C\dot{v}_{n-1} \tag{3.8}$$

Since the phase of the Josephson junction determines its behaviour and is linked to the voltage drop across the junction itself, J-SIM makes an attempt at guessing the phase at the next time step resulting in a set of non-linear equations which can be solved not with the Newton-Raphson [1] but using the less computationally intensive fixed point method [96] which is much simpler but requires a good initial guess of the phase.

[1] The Newton-Raphson method is expensive because at each time step and each Newton iteration, an LU decomposition must be done in order to solve $Ax = b$. The Jacobian (Equation 3.3) needs to be updated during each iteration requiring a new LU decomposition.

3.1.1 J-SIM Implementation and Model set-up

Circuits in J-SIM are represented as a single `.js` file, where every component of the circuit is defined using a **name**, numbering to represent **nodes** and a **value** taking the form `NAMEXXXX N1 N2 VALUE`. Capacitors, resistors, inductors and Josephson junctions are denoted as `C`, `R`, `L` and `B` respectively and take the input form `CXXXX`, `RXXXX`, `LXXXX` and `BXXXX`. Current `I` and voltage `V` are implemented as functions describing their behaviour. Sinusoidal, pulse or a piece-wise linear sources are given as `SIN`, `PULSE` and `PWL`, and they also require a `start`/`inital` values and times e.g. $V_{\texttt{bias}}$ `17 0 SIN(0 1MV 100GHZ 0US 0)` describes a sinusoidal voltage source named V_{bias} between nodes 17 and ground (0) with an initial voltage of 0, a maximum voltage of 1 mV a 100 GHz frequency, a delay of 0 and an a phase angle value of 0. A list of voltage and current source inputs are shown in Script 3.1.

```
Voltages
VXXXX N1 N2 SIN(Vint Vfin FREQ TD THETA)
VXXXX N1 N2 PULSE(V1 V2 TD TR TF PW PER)
VXXXX N1 N2 PWL(T0 V0 T1 V1 ....)
Current
IXXXX N1 N2 SIN(I0 IA FREQ TD THETA)
IXXXX N1 N2 PULSE(I1 I2 TD TR TF PW PER)
IXXXX N1 N2 PWL(I0 I0 T1 I1 ....)
```

Script 3.1: Example of Current and voltage inputs in JSIM. `SIN`, `PULSE` and `PWL` represent sinusoidal, pulse and piecewise linear inputs. Other inputs are TD= Total delay, TR = Total rise, Period width, FREQ = Frequency. All `PWL` sources must start with `V0` and `I0` at zero with an initial time `T0` of zero. All value inputs are either in decimal or scientific notation.

In addition to the above mentioned description of a Josephson junction they also must have a model specified which include junction critical current, capacitance, normal resistance e.g. `B1 1 0 myjj` describes a Joesphson junction named `B1` between nodes `1` and `0` with a model named `myjj` charactrised as `.model myjj jj(rtype=0,`

`rn=1000, icrit=100u, cap=0.25p)`. where `icrit` describes the critical current, `cap` is the junction resistance, `rn` is the normal resistance and the `rtype = 0` is specific for low T_c material, simulating high T_c substrates such as YBCO would require `rtype=1`.

Initial testing of J-SIM: In order to build a working model of our devices we first begin testing J-SIM using a single Josephson junction biased so that $I > I_c$, using the junction parameters reported by Oelze *et al.* [23] with a critical current $I_c = 340\ \mu A$ with an $I_c R_N$ product of 0.4 mV, the capacitance of the junction is calculated using Equation 1.44 so that $\beta_c = 0.1$. The JSIM script is described in Script 4.13.1.

```
* Capacitance of junction calculated for βc = 0.1

* Current source
Iinput 0 1 PWL( 0 0 100P 0 10PS 600uA)

*The Josephson junction and its model
B1 1 0 jjj0
.model jjj0 jj(rtype=0, rn=1000, icrit=340u, cap=0.06994063974173338PF)

*Shunt Resistor
R1 1 0 1.1764705882352944ohm

*Time Step and length of simualtion
.TRAN 0.1PS 1NS

.file B1_I_600.TXT

.print devv Bg
.print devi Bg
.print phase Bg
```

Script 3.2: JSIM script describing a single Josephson junction `B1` with critical current $I_c = 340\ \mu A$, shunted by a resistor `R1` biased by a current source I_{input} which are all connected between nodes `1-0`. The current source I_{input} has initial values of 0 a total delay of 100 ps after which the current rises from 0-600 μA in 10 ps, and is set at 600 μA to ensure that the Josephson junction is in the resistive state.The `.TRAN` statement a "transient analysis specification statement" and it dictates the output intervals and final time point of data. The final print statements output the voltage, current and the phase of the junction to a file titled `B1_I_600.TXT`.

Figure 3.1 shows the JSIM output compared to the numerical solution of the

RCSJ model which was obtained by solving the RCSJ Equation 1.39 using a python script that utilises a backwards Euler method with an initial guess of zero for the phase and a similar time step to that used in the JSIM model.

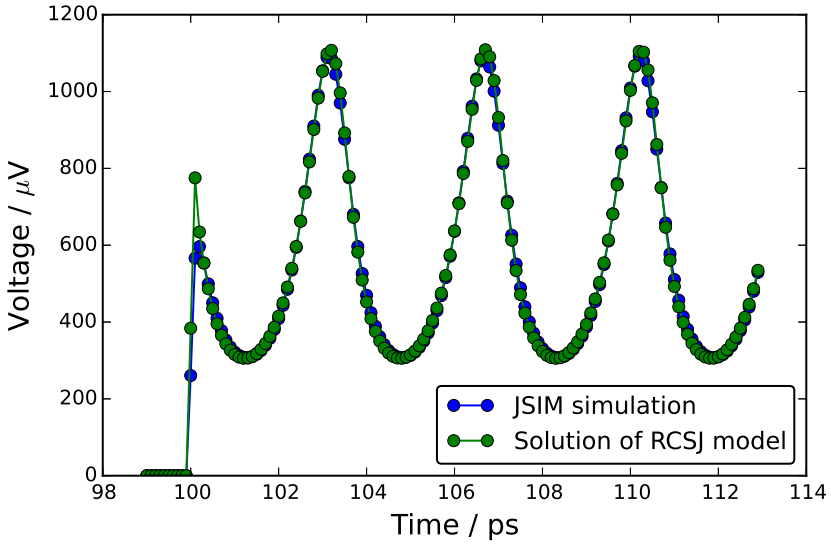


Figure 3.1: A segment of a 1 ns J-SIM time domain voltage simulations tested against the numerical solution of the RCSJ model described in Equation 1.39. The current source in both JSIM and the python script is set to $I = 600\ \mu A$. Both J-SIM and the numerical solution of RCSJ model are in good agreement during voltage rise periods they diverge slightly from each other during the fall of the voltage oscillations. This can be attributed to the inability to finely tune the current ramp time in our python program to that of JSIM.

Comparing V_{DC} over 1 ns for both, JSIM simulation and the numerical solution of the RCSJ model gives: 525.89 μV and 525.95 μV respectively, giving a 0.6 μV difference between the two. This can most likely be associated with the inability to finely match the current ramping rate in the python program to that of JSIM. Nonetheless this is an encouraging result and allows the focus to shift towards generating IV graphs.

Time step: As mentioned before, the power of J-SIM lays in its ability to reduce computational cost[2] when calculating the time step integration allowing it to preform calculations at much lower time steps compared to JSPICE where a 0.2 ps integration step lower limit is imposed. Figure 3.2 shows a J-SIM output of a single Josephson oscillation at different time step integration values using Script 4.1 and only altering the time step line of `.TRAN 0.1PS` the simulations are run for 1 ns and voltage comparisons are shown in Table 3.1.

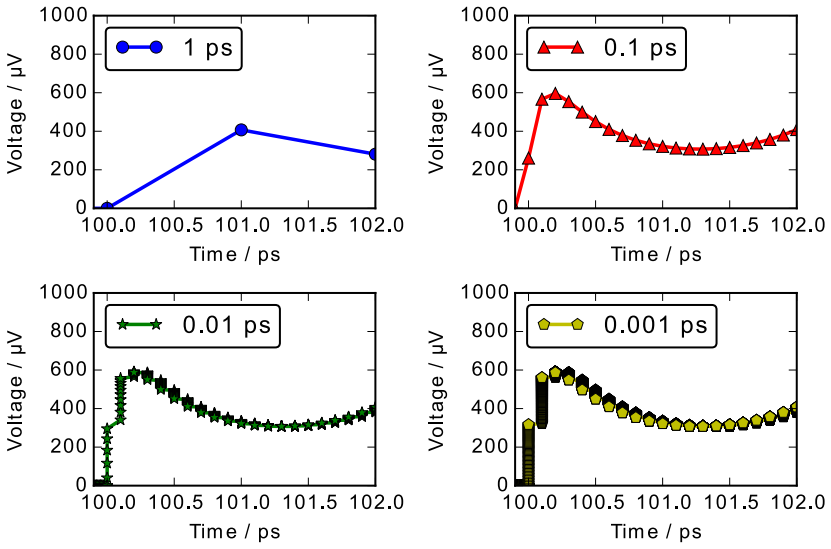


Figure 3.2: J-SIM output of single Josephson voltage oscillation at different time step. Using Script 4.1 and only altering the "Time step and length of simulation" and running simulations with `.TRAN 1PS`, `.TRAN 0.1PS`, `.TRAN 0.01PS`, `.TRAN 0.001PS`. A comparison between the different time steps is shown in Table 3.1.

Time step	V_{DC} / μV
1 ps	532.3763
0.1 ps	525.8856
0.01 ps	525.6944
0.001 ps	525.6884

Table 3.1: J-SIM voltage output of different time step simulations averaged over 1 ns from Script 4.1.

[2]The use of the iteration method instead of the Newton-Raphson method and the lack of requiring further LU decomposition allows J-SIM to significantly reduce calculation time allowing it to perform simulations at much lower time step something which is not possible with JSPICE.

Comparison between the different time 0.1, 0.01, and 0.001 ps shown in Table 3.1 reveals very little difference between the V_{DC} values of the J-SIM outputs. Since the simulations are done over a nanosecond and decreasing the size of the time step results in longer computation time, maintaining a 0.1 ps time step is a good compromise between accuracy and speed with only a 0.1912 and 0.1972 μV difference between the simulations of `.TRAN 0.1` and those of `.TRAN 0.01` and `.TRAN 0.001`.

Automation: Since J-SIM is a stand alone programme with no GUI (General User Interface), scripts must be written to automated the process of generating large numbers of `.js` files for processes such as creating IV graphs. Using python, a `.master` file is created, acting as a template it can be edited to change the current value of each `.js` creating the effect of a current sweep, the output is then processed again using python and in particular the scientific libraries of *Numpy*, *Scipy* and *Matplotlib*. An example J-SIM IV graph output is shown in Figure 3.3.

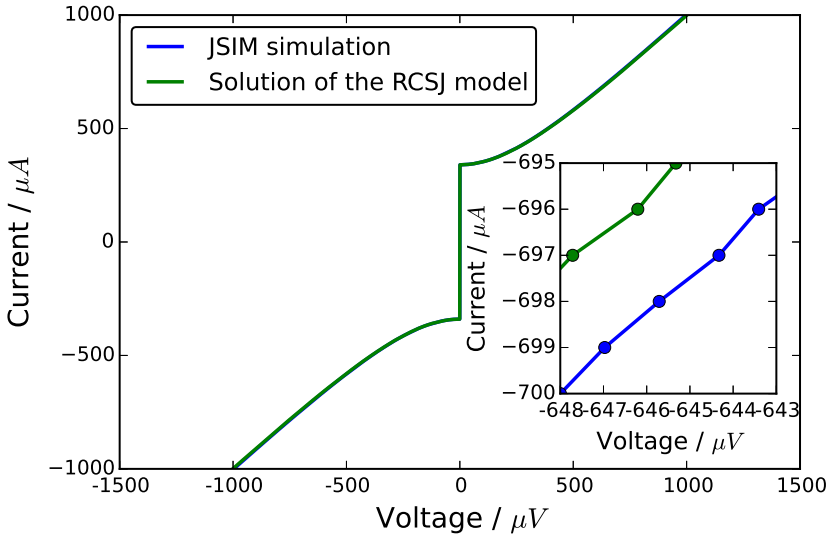


Figure 3.3: IV curve of J-SIM simulations of a single Josephson junctions described in Script 4.1 and the RCSJ solution of the same junctions. In both simulations the current source I_{input} set to sweep between -1000 to 1000 μA. Both the J-SIM and numerical solution of the RCSJ model give exactly similar IV graphs to each other, however closer inspection of a segment of the IV curve as shown in the inset shows that they diverge slightly. The total difference between theoretical and simulated error between the J-SIM output and the RCSJ model is $< 1\%$.

Noise: Through the addition of Gaussian distributed random numbers $\xi_i(t)$ and with zero mean and unit variance Julian Satchell [95] modified the original J-SIM circuit Equation 3.1 making the substitution:

$$F_i\left(x,t\right) \longrightarrow F_i\left(x,t\right) + \frac{g_i \xi_i(t)\sqrt{2}}{\sqrt{\tau}} \tag{3.9}$$

where the x_i, are the circuit variables, F is a (nonlinear) function of those variables, g_i are constants and τ is the total noise strength and is usually equated to $\sqrt{2}$.This substitution introduces random numbers at the start and the end of each time step, Julian Satchell recorded a 2% error between J-SIM simulations and theoretical models described by Ambegaokar and Halperin [95]. The actual implementation of noise is done as additional current sources in parallel to every resistors with a current spectral density shown in Equation 3.10. An example of a J-SIM model where noise is added at $T = 40$ K is shown in Script 3.3 and the accompanying IV graph in Figure 3.4 compares the J-SIM output with that from Equation 1.53.

$$S_i^{\frac{1}{2}} = \sqrt{\frac{4k_BT}{R_n}} \tag{3.10}$$

```
* Capacitance of junction calculated for βc = 0.1
* Current source
Iinput 0 1 PWL( 0 0 100P 0 10PS 600uA)
*The Josephson junction and its model
B1 1 0 jjj0
.model jjj0 jj(rtype=0, rn=1000, icrit=340u, cap=0.06994063974173338PF)
*Shunt Resistor
R1 1 0 1.1764705882352944ohm
*Thermal noise added as a current source across resistor
R1NOISE 1 0 NOISE(43.332232437297748P 0.0P 0.1P)
*Termination
.TRAN 0.1PS 1NS

.file B1_I_600.TXT

.print devv Bg
.print devi Bg
.print phase Bg
```

Script 3.3: The modified J-SIM script with the addition of thermal noise highlighted in green represents a thermal noise at $T = 40$ K.

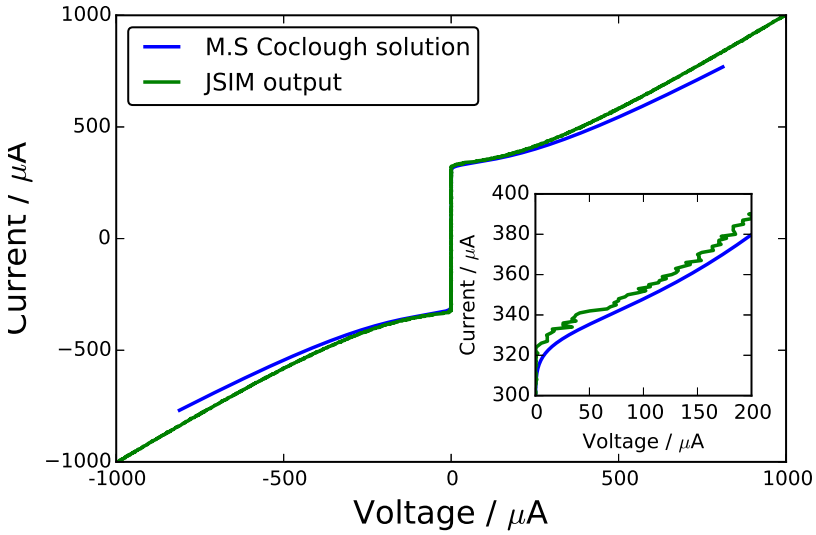


Figure 3.4: IV graph of Josephson junction described in Script 3.3. The numerical solution of the of M.S Coclough from Equation 1.53 is plotted against the J-SIM output. Noise is added at T = 40 K.

As powerful a tool J-SIM is, it can not be used as a single tool for circuit simulations as it requires prior knowledge of circuit parameters, whilst the I_cR_N product can be estimated to a high degree of accuracy using the KO (I) theory from Equation 1.55 in nanobridge Josephson junctions and the capacitance can be estimated from a predefined value of β_c in Equation 1.44, calculating the inductance of a circuit on the other hand require the use of simulation software.

3.2 Inductance estimation

Inductance estimation is an important step the superconducting circuit design. Example of tools used for inductance calculation are “L meter" [101] and the more popular “FastHenry” [102]. Application of “L-meter” suffers from difficulty in data input representation and time consuming computations, whilst “FastHenry” treats all structures as horizontal or vertical microstrips and therefore introduces errors when structures have curves and corners. The idea behind the development of 3D-MLSI specifically focused on solving these issues in superconducting structures and “revolves around simplifying the input process hence allowing the user to

define general structures as needed and ensuring fast and accurate calculations of inductance in any 3D structure." [103].

3.2.1 3D-MLSI

3D-MLSI can simulate both high and low T_c superconducting structures fabricated from thin superconducting films. It is possible to simulate self and mutual inductances for currents circulating around the holes and for variety of other designs. Figure 3.5 is a task flow chart for the program.

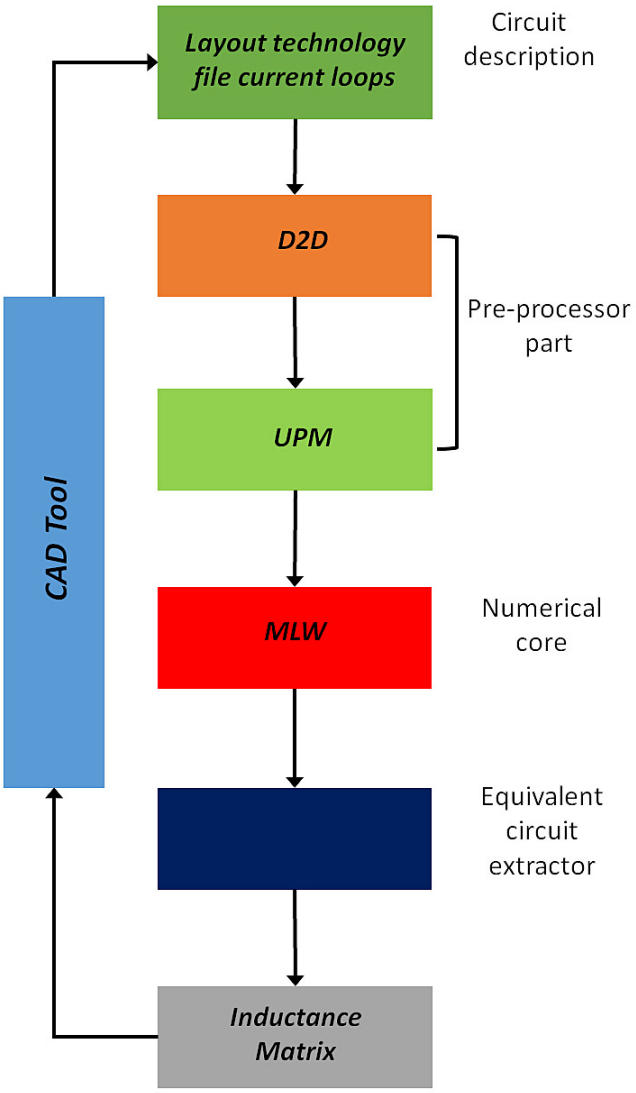


Figure 3.5: Flow chart of the different steps 3D-MLSI undertakes to prepare the finite element matrix used to solve the inductance of superconducting devices.

Implementation: The input of 3D-MLSI allows for the interactive drawing, editing of current paths and terminals, and the importing of calculated inductances into the schematic. Its CAD input takes a `.txt` or `.dat` file with x and y coordinates in addition to some other properties of the superconducting structure e.g. London penetration depth, film thickness and the number of conducting layers present. Currents can either be induced by the magnetic flux trapped in holes of the films, induced by external magnetic field or inputted through predefined terminals. An example of a 3D-MLSI file is shown in Figure 3.6.

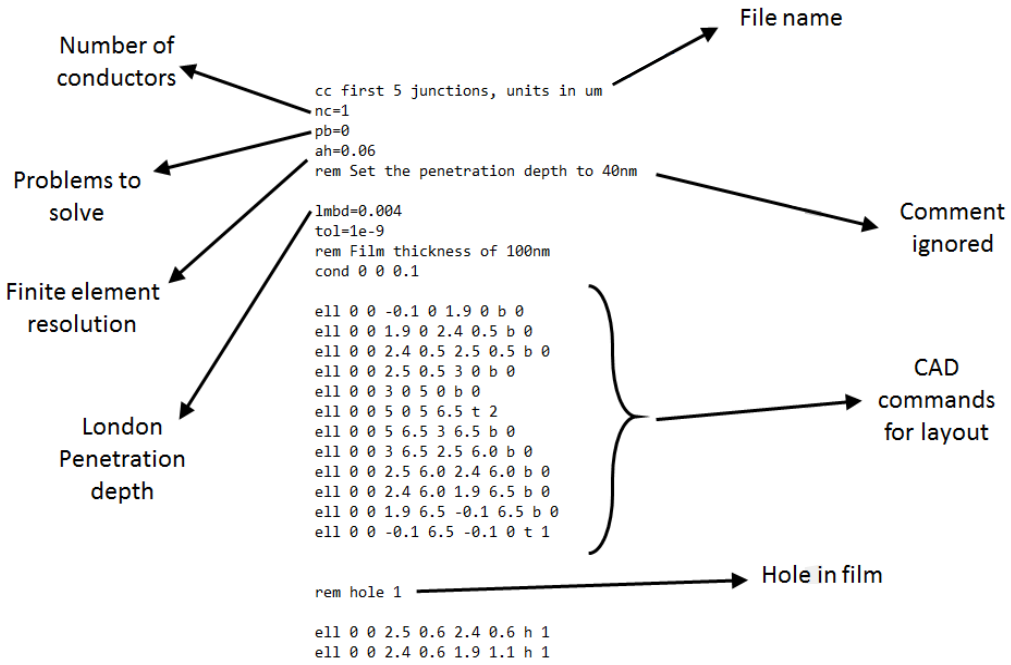


Figure 3.6: Example of an input file in 3D-MLSI.

UPM and MLW: 3D-MLSI consists of a pre-processor (**UPM**) which takes CAD input and is responsible for the creation of the finite volume mesh used in the numerical core. Successful execution of **UPM** creates two files: `name.upm` which contains various data and `name.trg` which contains triangular mesh. The triangular mesh is very important in the calculation of inductance by (**MLW**), the finer the mesh (more triangles present) the more accurate the inductance calculation from

the numerical core (**MLW**) is. As input, (**MLW**) takes the two files generated by (**UPM**): `name.upm` and `name.trg`. When executed successfully (**MLW**) creates a further two files: `name.psi` (solution) and `name.out` (inductances or other specific data). An example of the output generated from (**UPM**) and (**MLW**) file are shown in Figure 3.7.

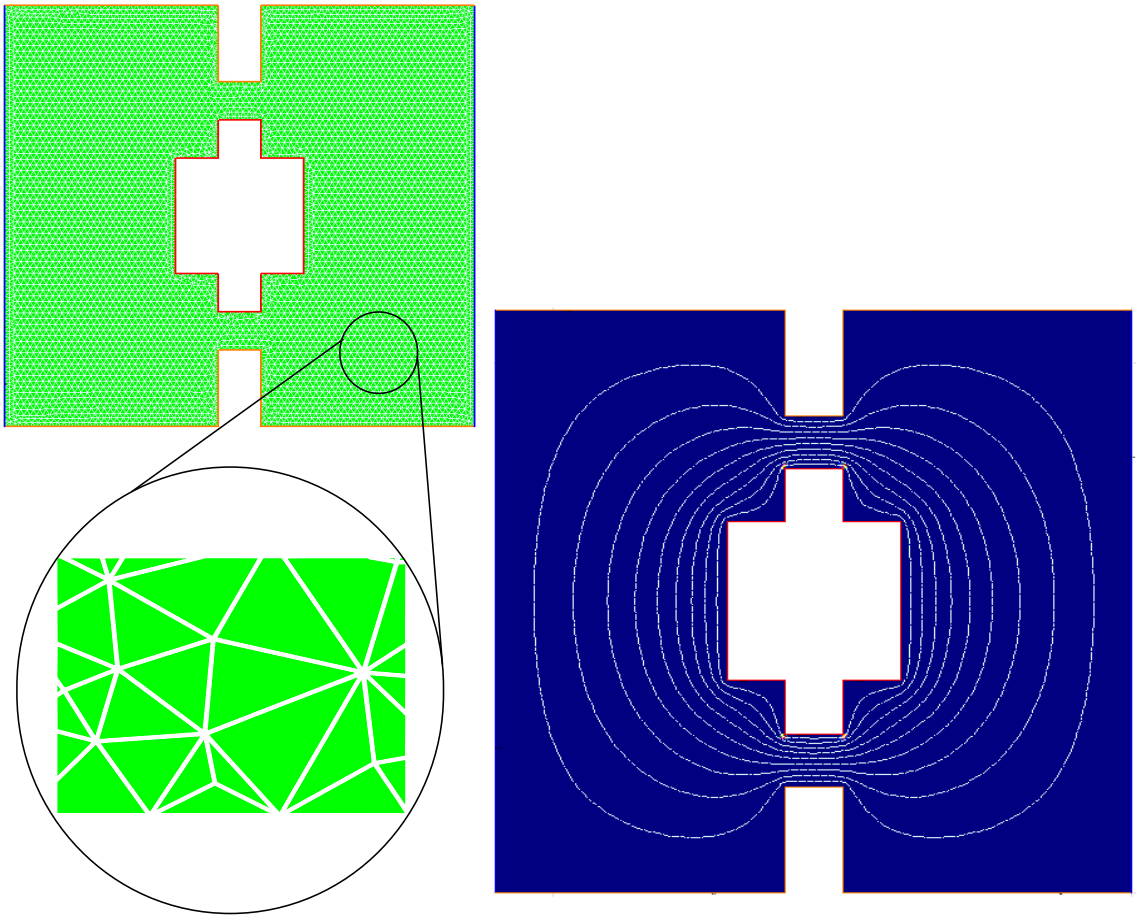


Figure 3.7: An example of a 3D-MLSI simulation of a small SQUID with the circulating current shown. The first image shows the (**UPM**) output with the triangle mesh highlighted in the inset. Whilst the second image shows the output from (**MLW**) with the induced current lines shown in white.

3.3 Overview of techniques for nanobridge fabrication

3.3.1 Lithography

Lithographic processes are usually split into i) photolithography, and ii) nanoscale lithography such as electron beam lithography. In research labs both techniques are usually reserved for specific process e.g. photolithography is normally used to pattern μm sized contact pads and tracks, whilst electron beam lithography is set aside for sub-μm structures and therefore is very vital in the fabrication of nanobridge weak links.

Photolithography: One common technique in photolithography employs resist lift off. Using a Lift-Off Resist (LOR) which is spun on a wafer and then baked after which a positive or a negative photo resist is then spun on top and is baked again forming a bilayer. The coated resist is then exposed with ultraviolet light through a manufactured chromium mask, the UV light breaks the chemical bonds of the resist molecules making it soluble in photo-resist developers such as MF-26, a TMAH-based (Tetramethylammonium hydroxide) developer. If the resist is positive then the exposed areas are removed whereas if the resist is negative then the opposite case is true and the unexposed areas are removed. In both cases the presence of LOR results in an undercut since it is more sensitive than the other resist. As this method is reserved for micron sized structures such as contact pads and tracks, highly conductive materials are then thermally evaporated on to the wafer. in this particular example Chromium is used as a non-magnetic adhesion layer and gold usually provides a stable, highly thermally and electrically conductive layer. Excess metal and photo resist and LOR are then removed in lift-off through an acetone bath and sonication.The process is summarised in Figure 3.8.

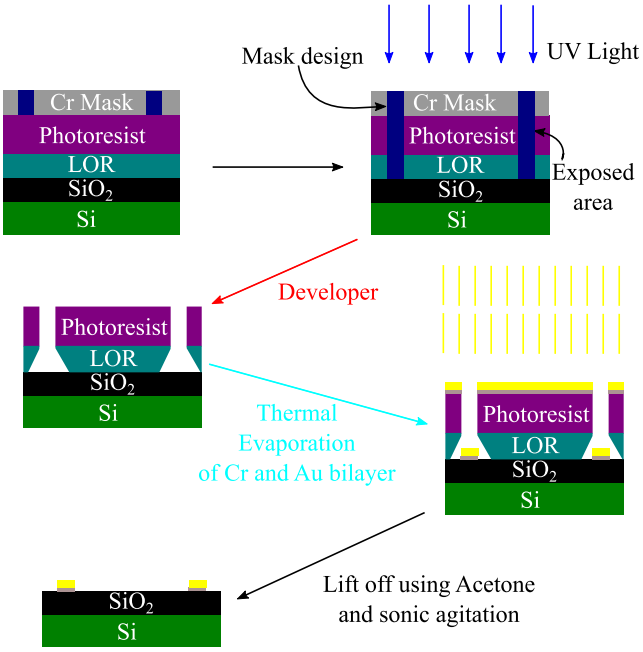


Figure 3.8: Graphic illustration of the photolithographic lift off process using *LOR* and a positive photo resist followed by development and the thermal evaporation of Cr and Au.

Electron-Beam Lithography: Photolithography is a very effective method for micron scale structures but due to the nature of weak links and the Josephson effect sub-nm structures are required, this is only possible with Electron Beam Lithography (EBL) or some other nanoscale processing technique. Derived from the early scanning electron microscopes, EBL is a specialised technique for creating sub-nm structures required by the modern electronics industry for integrated circuits. The main attributes of the technology are i) its capabilities of very high resolution and ii) its flexibility allowing it to work with a variety of materials and realise an infinite number of patterns.

Electron Beam Lithography relies on a controlled beam of electrons to expose a section of resist. The incident energy available ranges from a few hundred electron volts to 100 keV. Electrons can be focused either by electrostatic forces or magnetic forces. Electron lenses in principle behave the same way as optical lenses in all but a few special cases. The quality of electron lenses are not nearly as good as optical

lenses in terms of aberrations. In an EBL system, one set of lenses controls the aperture and therefore the current of the beam. Another set of lenses blanks the beam to protect the sample from unwanted exposure during idle time. Finally, some demagnifying lenses and some deflectors steer the beam exactly to the required position. The general set-up is shown Figure 3.9.

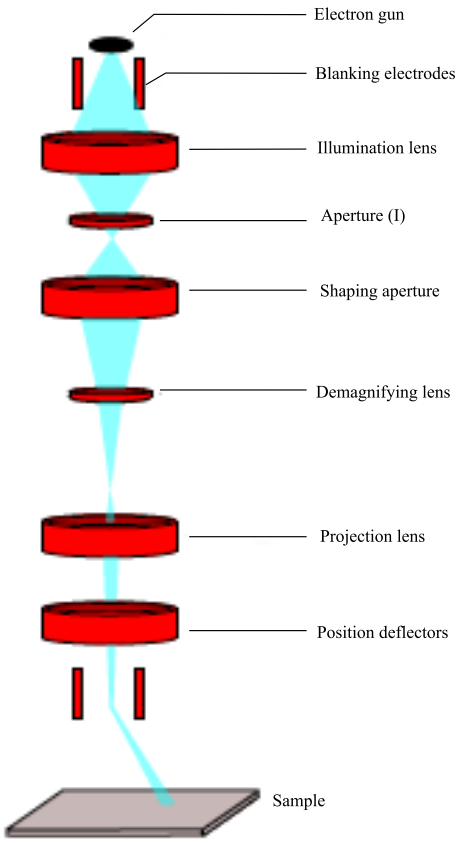


Figure 3.9: An example for a typical EBL set-up found in many clean rooms.

Film deposition: Metallisation or film deposition of superconducting thin films can be achieved through techniques such as electron beam (e-beam) evaporation or magnetron sputtering. Depending on the desired metal one method is more favourable than the other. E-beam evaporation is ideal for films with relatively low evaporation temperature such as aluminium, gold and titanium, whilst malleable metals that are difficult to evaporate in e-beam systems such as refractory metals e.g. niobium or complex alloys generally require sputtering to achieve high quality

films.

Electron beam evaporation uses energy transfer by heating a crucible filled with a target material, by bombarding it with electrons generated from a tungsten filament. This causes the atoms of the target material to evaporate into the gaseous state, after which they precipitate into solid form and coat everything in the chamber included a substrate such as a silicon wafer (resting within line of sight) with a thin layer of the target material. A crystal monitor usually placed near the sample records the thickness of the film. In sputtering however, the process involves the use inert ionised gas (usually argon) to eject material from a target acting as a source onto a substrate such as a silicon wafer in a vacuum chamber.

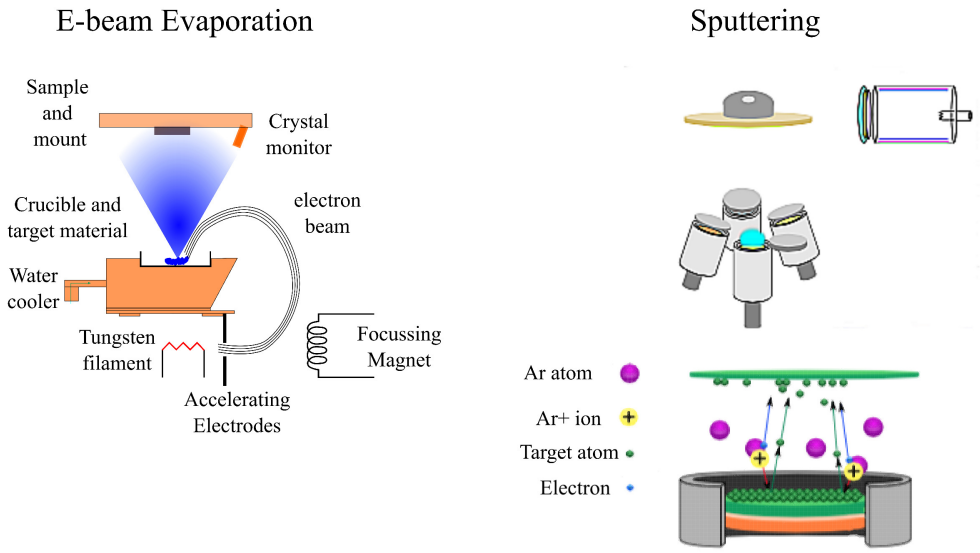


Figure 3.10: Schematic representation of the different methods of metallisation. On the left a typical set-up of an e-beam evaporator system is shown. The focusing magnets bend the electrons generated from the tungsten filament onto the crucible containing the target material causing it to evaporate and precipitate into solid form and coat the sample. A crystal monitor is used to track the thickness of the films deposited allowing the system to be automated by shutting down the source once a desired thickness is reached. On the right an example set-up of a sputtering system using Ar atoms that are ionised and accelerated towards the target causing atoms to be ejected and deposited on to the sample. Image of sputtering system adapted from PhD thesis of Arnaud Blois [104].

Once the pattern is transferred successfully on to the resist and depending on when the metallisation of the substrate occurred i.e. before the application of the e-beam resist or after the development of the resist, two possible methods are available for the realisation of a nanobridge structure.

Lift-off and Etching: Based on opposing principles, much debate in literature has surrounded the efficacy and superiority of lift off and etching compared to one another. The e-beam lift-off process follows the same principle as was seen in photolithography (see Section 3.3.1) where after development of patterned resist and metallisation, excess resist and thin film are removed by a mild solvent usually acetone and sonication leaving only the metal in the opening of the resist that has adhered to the wafer. In the etching process, the metal film is deposited first followed by the e-beam resist which is then patterned. After successful transfer of the pattern, both resist and metal are etched down to the desired structure after which the resist is stripped off. Figure 3.11 gives a brief overview of the two different techniques.

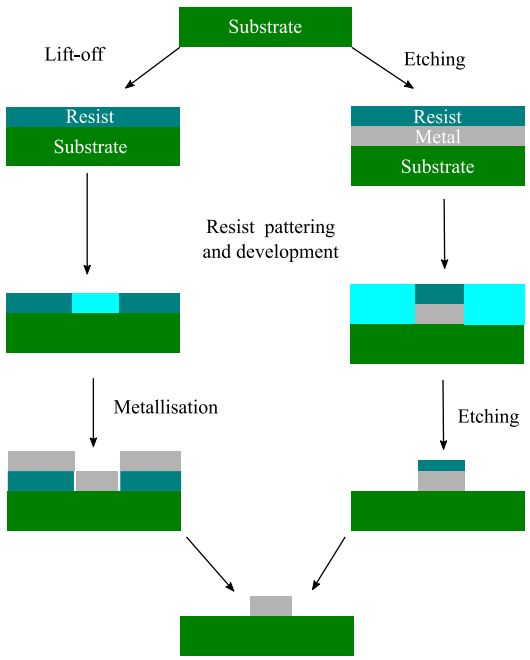


Figure 3.11: A schematic representation of the additive lift-off process and the subtractive etching method.

Etching of the sample can be achieved through techniques such as argon milling or Reactive Ion Etching (RIE). Both procedures involve the deposition a resist on top of a metal and then removing both the exposed resist and the metal underneath that region to only leave the desired structure.

Reactive Ion Etching and Argon Milling: Fabrication of Nb nanobridges is well documented in literature using etching processes. The most commonly used techniques for the realisation of sub μm structures are argon ion milling and Reactive Ion Etching (RIE). In argon ion milling, gaseous argon atoms are ionised and accelerated towards a sample via an electric field generated by an acceleration grid, before collisions with the sample occur the argon ions are deionised through an electron emitting grid usually referred to as neutralising grid regenerating the argon atoms and in the process generating a wide beam that etches everything that is exposed to it. There is a variation in the etching rate of material e.g target metal etches at a rate 3 to 10 times faster than the e-beam resist. So while everything etches to some degree, when the process is complete, the metallisation that defines the circuit remains.

RIE on the other hand is a mix between a physical and a chemical etch, employing an RF field to generate plasma that strips electrons from heavily electrophilic atoms such as SF_6 and CF_4 creating positively charged ions which accelerate towards the sample due an electric field generate from two electrodes in in the chamber. The ionised atoms start etching down the exposed area of the resist and the metal underneath, leaving only the desired structure. A schematic representation of both processes is given in Figure 3.12.

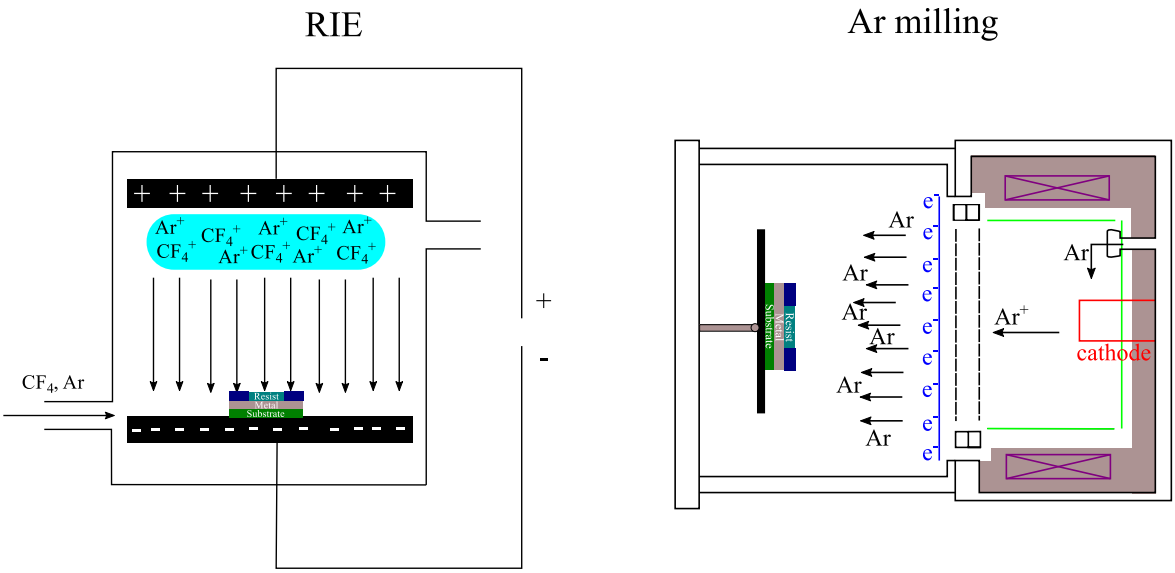


Figure 3.12: Schematic diagram of both RIE and argon milling. The image on the left is a simplified example of RIE using CF_4 and Ar which are inject into a chamber in gaseous form where plasma (blue) strips electrons from them creating positively charged ions which accelerate towards the sample due to the electric field generated from two electrodes. Whilst in argon milling, argon gas is introduced into a chamber where a combination of a heated cathode (red), anodes (green) and magnetic field generated from solenoids (purple) ionises the argon atoms at which point they optically aligned grids extract highly ionised Ar^+ and direct it towards a Neutraliser (blue) which reforms the Ar atoms resulting in a fully neutralised ion beam that mills down the resist and a small amount of the thin film.

3.3.2 Techniques for realisation of nanobridge weak links

EBL and resist: Although electron beam lithography tools are capable of forming extremely fine probes, the main factor limiting the resolution is the resist. Ideally, an e-beam resist should have both a high contrast and a high sensitivity but in practice they are often conflicting. There is a very wide range of e-beam resists: organic or inorganic, chemically amplified or not. However, despite being one of the first resists to be discovered in 1968, Poly(MethylMethAcrylate) (PMMA) still provides the best performance. Sub-100 nm features are routinely achievable by lift-off. As the electrons penetrate the resist, they experience many small angle scattering events (forward scattering), which tend to broaden the initial beam diameter. As the electrons penetrate through the resist into the substrate,

they occasionally undergo large angle scattering events (backscattering). The backscattered electrons cause the proximity effect, where the dose that a pattern feature receives is affected by electrons scattering from other features nearby. During this process the electrons are continuously slowing down, producing a cascade of low voltage electrons called secondary electrons.

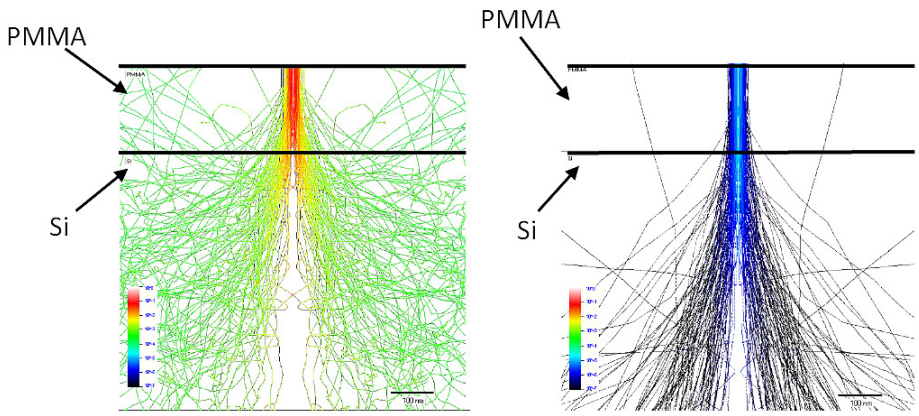


Figure 3.13: Monte-Carlo simulations of the electron scattering for two different acceleration voltages on a 200 nm thick PMMA layer. The image on the left represents the beam simulation at 10 keV, the low beam energy is represented in the green and red colours of the lines. The image on the right with deep blue colours is that of a 30 keV beam. The 30 keV beam suffers less forward and backscattering resulting in better defined lines.

Figure 3.13 shows a Monte-Carlo simulation of the electron trajectories through 300 nm of PMMA using the Raith simulation software included with the EBL system in the London centre for nanotechnology (LCN) at 20 keV and 30 keV respectively. It is clear that a higher beam energy results in less scattering. Though each interaction only deviates electrons by a small angle, they are very frequent which can lead to a wide diffraction angle, especially at lower beam voltages. A higher beam energy results in less scattering but more damage to the substrate. A bigger aperture leads generally to better images and a better signal to noise ratio but comes at the cost of a smaller depth of focus, a lower resolution and more damage to the sample due to higher current values.

An alternative to EBL that some groups have used to pattern nanobridges is utilise a Focused Ion Beam (FIB) as the main writing process to acheive the desired nano scale structure. Using photolithography for the μm sized structures and an FIB for sub-μm features means complex devices can be obtained in very few steps.

Focused ion beam: FIB utilises a beam of ionised elements (usually gallium) fired from a gun to bore down into a sample, as the ions hit the surface of the sample material a small amount of the metal is sputtered as secondary ions (i.e. M^+ or M^-) and in the process producing some electrons which when collected to form an image of the substrate. Figure 3.14 shows a simple illustrative set-up of a Ga/FIB. The disadvantage of FIB is that it results in Ga^+ implantation in the edges of the superconducting film which poisons the material reducing its transition temperature or destroying superconductivity all together.

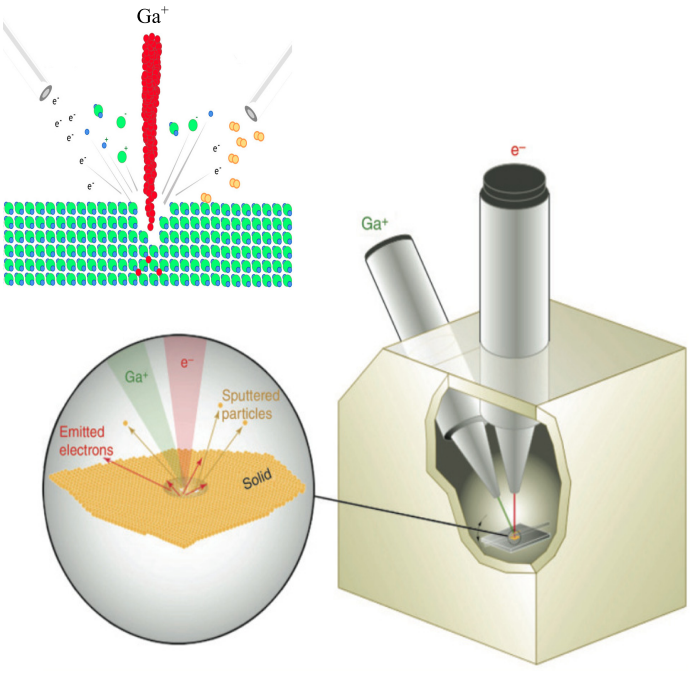


Figure 3.14: Simplified set-up of a Ga/FIB system. A Ga^+ gun fires Gallium ions towards a substrate which bore into the sample as shown in the inset, resulting in some material begin sputtered as either secondary ions or atoms and emitting electrons which are collected and used to form an image of the substrate.

3.4 Review of work on niobium nanobridge weak links in the literature

EBL: Much of the early work revolving around the fabrication of Nb nanobridge weak links relied on the use of e-beam lithography in addition to a milling, etching or lift-off process [38, 105–107]. An example of a process used to successfully realise Nb weak links is by Tachiki *et al.* [108] who fabricated and tested 20 nm thick Nb weak links with a minimum bridge area of 65 nm and 60 nm in width and length respectively. The ideal Josephson effect was observed for all samples that had a width of < 110 nm. The devices were realised through the use of a 80 kV and 204 C/cm^2 EBL recipe to pattern a sample of a positive e-beam resist overlaid on top of a 20 nm thick Nb thin film, the resulting structure was then etched using CF_4 and O_2 gases in a 90-10% mixture, with voltage acceleration and current density of 400 V and 1.05 mA/cm^2 respectively. One of the successfully fabricated Nb weak links and a measured IV curve are shown in Figure 3.15.

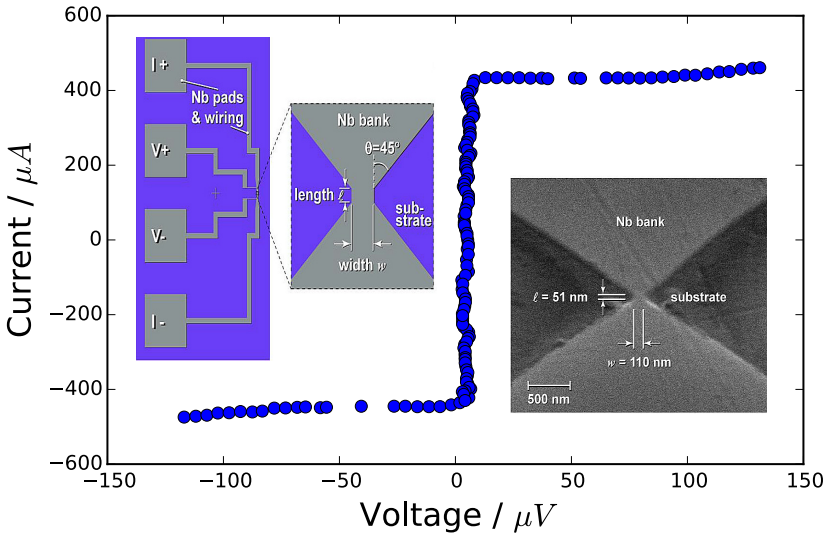


Figure 3.15: Design and SEM image of a 20 nm thick Nb weak link with T_c of 8.4 K, $\ell = 51$ nm and $w = 110$ nm. The measured IV graph of the fabricated nanobridge is shown at $T = 7.1$ K. Adapted from Tachiki *et al.* [108].

FIB: A lot of work has been done into fabricating nanoSQUIDs using Ga/FIB by Hao *et al.* at NPL [109–113]. An example of two devices is shown in Figure 3.16. Fabrication of this device starts with sputtering of 100-200 nm thick Nb film on to an oxidised silicon wafer. Standard photolithographic technique were used for the larger structures such as tracks whilst a dual beam Ga/FIB system from Nova Nano-lab[3] was used to produce the nanobridges. The beam current was kept to about 10 pA so as to minimise beam size and allow very small structure to be fabricated. The group has also recorded T_cs of between 6-9 K depending on the degree of Ga^+ implantation. An example of the temperature dependence of the measured critical current for the two devices in Figure 3.16 is shown in Figure 3.17.

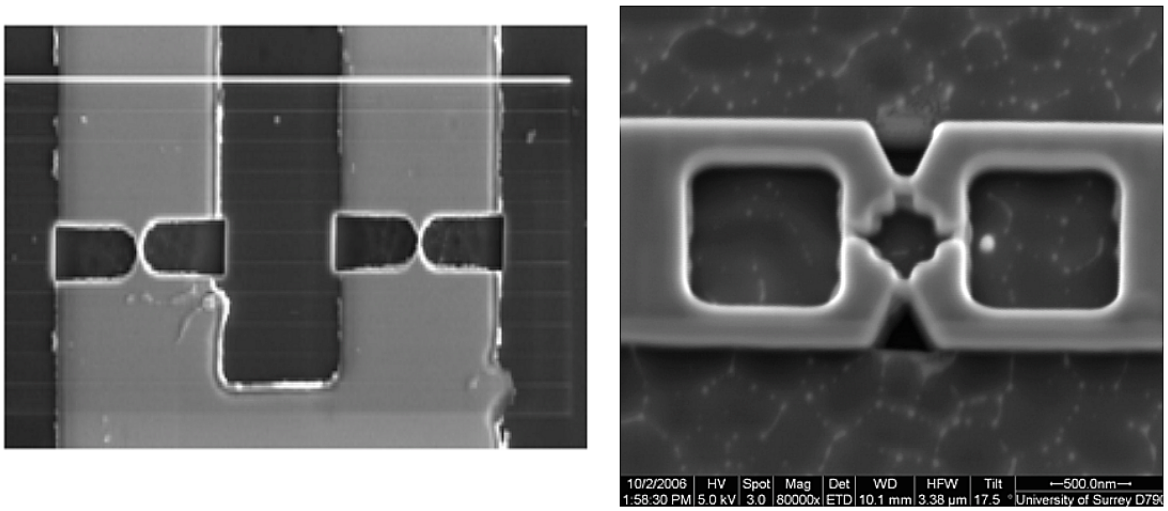


Figure 3.16: SEM images of two nanoSQUIDs fabricated by NPL with dimensions of 65 nm width for the structure on the left and a proof of concept for the dual beam system through the fabrication of the structure on the right, a tri-loop SQUID which are very difficult to obtain through traditional EBL methods. A Co particle (the white dot in the right hand loop) was also deposited within that loop. Adapted from Hao *et al.* [113].

[3]The Nova Nano-lab FIB used by *et al.* in this example is capable of nanoscale structures down to below 50 nm

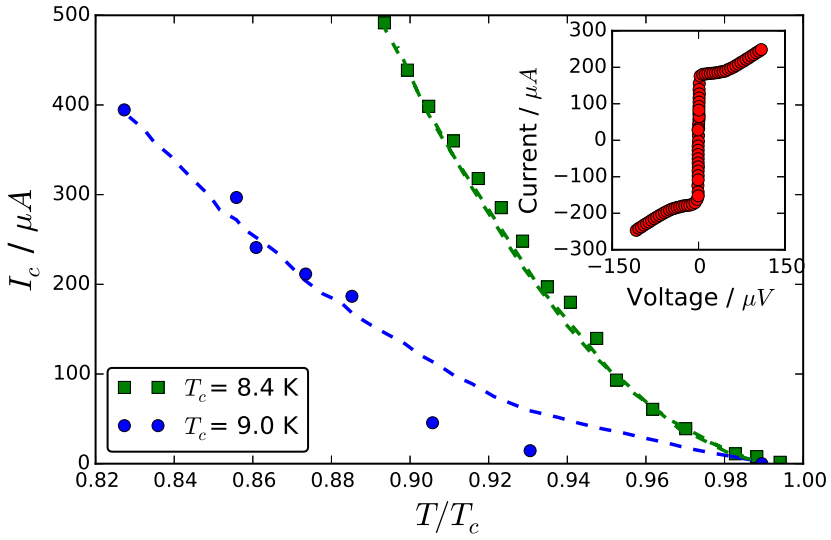


Figure 3.17: Graph of the temperature dependence of I_c in two samples measured by NPL. I_c data fit is set to $I_c \propto (1 - T/T_c)^2$, which is predicted by a number of models including the thermal phase slip predicted in Ambegaokar and Halperin model (see Section 1.2.1) and is observed in a number of Josephson junction devices, a more in-depth analysis can be found in [38, 114]. Adapted from Hao *et al.* [113]

Typical transition temperatures for Nb thin films tend to be between 8-9 K, which is the same measured for nanoscale Nb structures fabricated through EBL methods. However the T_c of Ga/FIB fabricated nanoscale devices tends to vary quite considerably as is seen in the work of Hao *et al.*. This is due to Ga ion implantation as is seen in in the inset of Figure 3.14 which result in the poisoning of the superconducting thin films. This leads to lowering in T_c or even destroying superconductivity. It can also lead to contamination of the underlying structure and even create defects in thin films over great lengths, up to 50 nm. The implantation depth in Nb can be between 30-40 nm which is why it becomes a significant issue for structures smaller than 100 nm. Recently introduced neon or helium-ion FIBs have been shown not to suffer from these drawbacks and as such have been showing great promise in the field of nanoscale fabrication and can be looked at as a genuine alternative to both Ga/FIB and EBL methods.

Chapter 4

Initial testing and model set-up of RSFQ circuit in JSIM

4.1 Introduction

As mentioned previously the true measure of the performance of a Josephson comparators is the grey zone, which describes its decision uncertainty. In an ideal case this would be a Heaviside step function as shown in Figure 4.1.

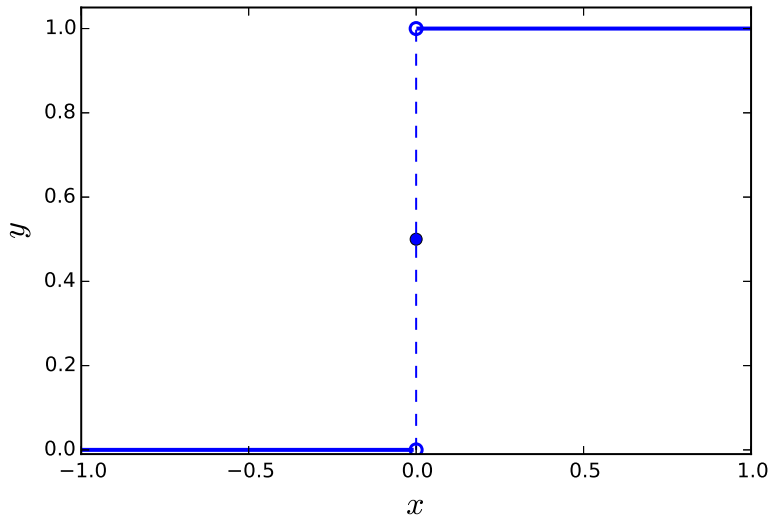


Figure 4.1: Illustration of a Heaviside step function. In a real device the transition will most likely appear spread over a region around $x = 0$.

As mentioned earlier there are several ways of defining the grey zone. However in this present work, since the transition edges are sometimes not ideal we have to use some alternative definitions and fits to the data:

- The current range ΔI_{x} corresponding to the switching probability between 0.1 and 0.9. This can be used in simple cases where the start/end of the grey zone is poorly defined.

- Another method is to use the approximation introduced by Haddad *et al.* [88] where the grey zone is defined as $\mathrm{GZ} = 1/m$ where m is the slope of the tangent at switching probability $p = 0.5$ of the switching probability curve.

Error and double error functions: As mentioned earlier the switching behaviour in an ideal Josephson comparator can be described by a Heaviside step function as was seen in Figure 4.1. This however is not true in real devices though since, due to the presence of thermal noise, the switching decision is not deterministic i.e. the transition between the states "0" and "1" is not a vertical step, instead the switching probability is spread over a region. This behaviour can be approximated numerically by an error function (erf) as shown in Equation 4.2, which is a modified Heaviside step function [87]:

$$\mathrm{ERF(I)} = \frac{1}{2} + \frac{1}{2}\mathrm{erf}\left(\sqrt{\pi}\frac{I_{\mathrm{x}} - I_{\mathrm{th}}}{\Delta I_x}\right), \tag{4.1}$$

$$\mathrm{ERF(I)} = \frac{1}{2} + \frac{1}{2}\mathrm{erf}\left(\sqrt{\pi}\frac{I_{\mathrm{x}} - I_{\mathrm{th}}}{\mathrm{GZ}}\right) \tag{4.2}$$

At high operational frequencies the Josephson comparator loop may start to store more than one flux quanta at a time before a decision is made by either comparator junction. This increase in uncertainty is especially prominent around the threshold current I_{th} which results in the formation of a plateau around that region as shown in Figure 4.2.

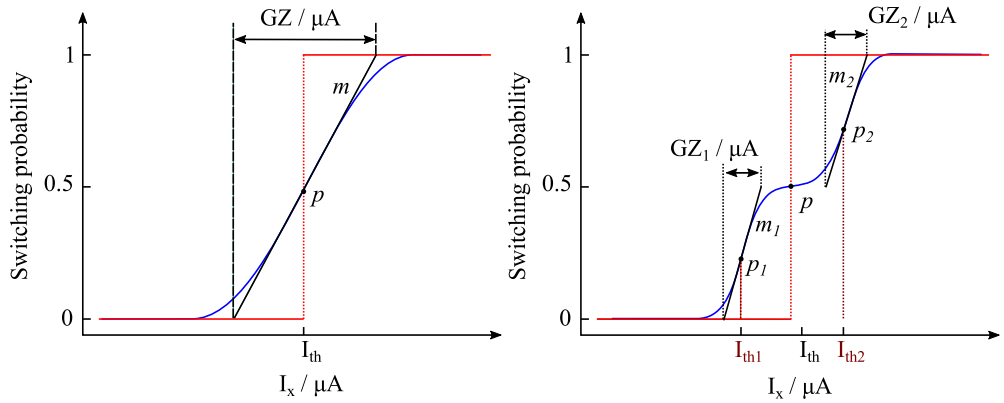


Figure 4.2: Schematic representation of the two error functions ERF(I) and ERF(II) shown on the left and right respectively. The difference of the threshold currents $I_{\mathrm{th2}} - I_{\mathrm{th1}}$ is a measure of the plateau present in the double error function.

The presence of the plateau results in an alteration of the numerical formula used to calculate the switching behaviour of the Josephson comparator. Instead of a single error function describing the switching behaviour as shown in the right of Figure 4.2, instead it can be fitted to a double error function, ERF(II), which is characterised by two threshold currents I_{th1} and I_{th2}, where I_{th1} and I_{th2} are represented as the currents at $p = 0.25$ and $p = 0.75$ respectively, and by two grey zone widths GZ_1 and GZ_2 [87]. This is given by:

$$\mathrm{ERF\ (II)} = \frac{1}{2} + \frac{1}{4}\mathrm{erf}\left(\sqrt{\pi}\frac{I_x - I_{\mathrm{th1}}}{\mathrm{GZ}_1}\right) + \frac{1}{4}\mathrm{erf}\left(\sqrt{\pi}\frac{I_{\mathrm{x}} - I_{\mathrm{th2}}}{\mathrm{GZ}_2}\right) \tag{4.3}$$

In an ideal scenario the threshold current $I_{\mathrm{th1}} = I_{\mathrm{th2}}$ and the grey zone widths $\mathrm{GZ}_1 = \mathrm{GZ}_2$ results in the switching probability curve being accurately represented by the single error function in Equation 4.2. Hence the double error function, ERF(II), reduces to the single, ERF(I). However when $I_{\mathrm{th1}} \neq I_{\mathrm{th2}}$ and $\mathrm{GZ}_1 \neq \mathrm{GZ}_2$ this will result in a double error function characterised by a plateau as shown in the second graph of Figure 4.2.

4.2 Comparator and JSIM set-up

Comparator: The device fabricated and tested by Oelze *et al.* [23] previously mentioned in Section 2.2.3 and shown in Figure 4.3 is an ideal candidate for testing the viability of using weak link nanobridge Josephson junction as the active element in an RSFQ circuit. The simplicity of the device means that it can be fabricated using low T_c material such as Nb, either patterned through an EBL or FIB method as described in Section 3.3.2.

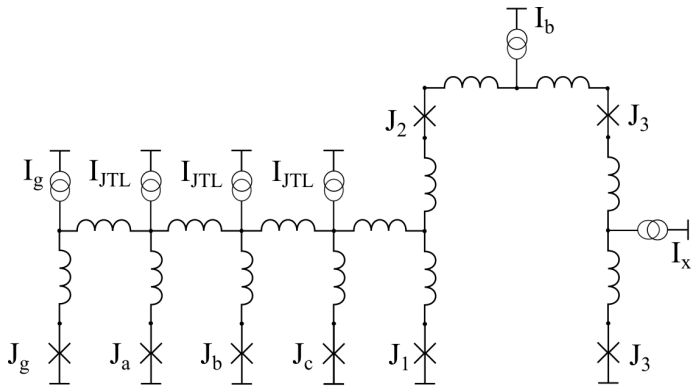


Figure 4.3: Circuit diagram of Josephson comparator designed by Oelze *et al.*. The junctions are labelled as J_g for the generator junction, $J_{a\text{-}b\text{-}c}$ denote the JTL junctions and finally the comparator loop consisting of $J_{1\text{-}2}$ acting as the buffer stage and junctions $J_{3\text{-}4}$ as the comparator junctions. As an SFQ pulse generated from junction J_1 travels through the circuit via the JTL junctions Ja-b-c and is introduced into the larger comparator loop via J_1, either junctions J_3 or J_4 will begin to oscillate depending on the value of the input current from I_x. The current biasing source I_b acts as balance and its role will be looked at in more detail in Section 4.3. Adapted from Oelze *et al.* [23].

Initial set-up and testing of JISM was performed using the junction parameters reported by B. Oelze *et al.* e.g. critical current I_c of 340 μA with an I_cR_N product of 0.4 mV at T = 40 K. In order for the Josephson junctions to function as RSFQ elements they must be non-hysteretic which leads to an assumption of a β_c value of < 1. Since the capacitance of non-hysteretic junctions is negligible we will take $\beta_c = 0.1$ to calculate the junction capacitance needed in the J-SIM model. The junction normal state resistances R_N were added as separate shunt resistors in the model. Noise sources were added at 40 K to each resistor.

4.2.1 Model set-up

The first process in designing and implementing the Josephson comparator in J-SIM is calculating the loop inductance and inductance distribution of the said circuit. The inductance distribution of the circuit we will be testing in this report can be broken into two main segments:

- The inductance loops of the Josephson Transmission Lines
- The inductance of the larger comparator loop

Oelze *et al.* fabricated and simulated the JTL loop as a hole with inner dimensions 2×5 μm as shown in Figure 4.4. The inductance distribution of the comparator loop on the other hand is somewhat more ambiguous due to part of the superconducting loop design begin masked by over layers in the published diagram, the reported value is of 24 pH. [23] .

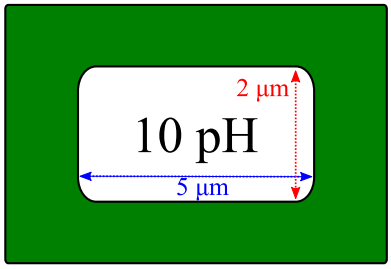


Figure 4.4: Graphical representation of the geometry used in the high T_c 3D-MLSI simulation of inductance of the JTL loop.

Inductance: Calculating the inductance of a superconducting structure requires the use of finite element tools such as 3D-MLSI, however for the sake of simplicity it is usually safe to assume that a superconducting loop increases with inner perimeter and is uniformly distributed throughout the loop. To ensue optimal current distribution inductors are split into several groups of equal values as shown in Figure 4.5.

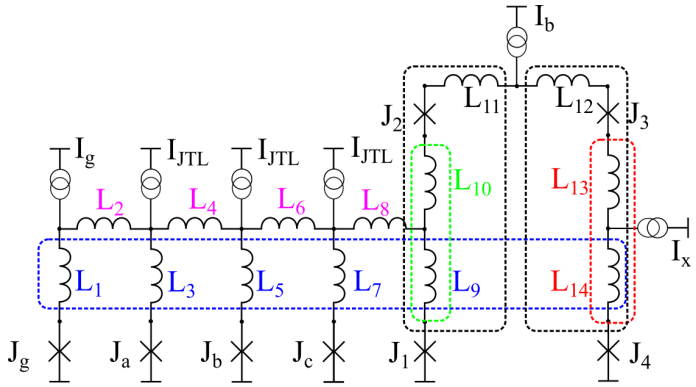


Figure 4.5: Circuit diagram of the comparator loop and lumped inductors which need to have equal values to ensure equal current distribution.

Since all the oddly numbered inductors of the JTL loop have the same inductance values and in order to achieve equal current distribution between both L_9 and L_{10} they must also have the same inductance values. Finally to ensure even current distribution of I_b results in $L_9 + L_{10} + L_{11} = L_{12} + L_{13} + L_{14}$ and since L_9 and L_{14} are connected though ground therefore must have an equal distribution so as to not create in miss timing of flux arrival from the JTL. This finally gives us an inductance distribution in the form of:

$$L_2 = L_4 = L_6 = L_8$$

$$L_1 = L_3 = L_5 = L_7 = L_9 = L_{10} = L_{13} = L_{14} \tag{4.4}$$

$$L_{11} = L_{12}$$

Using the relationships in Equation 4.4 and the total values estimated by Oelze *et al.* for high T_c material, we calculate the inductances as, $L_1 = 2.22$ pH, $L_2 = 5.56$ pH and $L_{11} = 7.56$ pH we estimate similar total values ourselves using 3D-MLSI.

Current source timing: The final section required to construct a working J-JSIM model concerns the timing of when bias sources are switched on. Script 4.1 describes the final model used to simulate the Josephson comparator in Figure 4.3.

```
* Capacitance of junction calculated for β_c = 0.1 and Noise is added at 40 K
* Current source
Iinput 0 1 PWL( 0 0 100PS 0 10PS 520uA)
Ijtl1 0 3 PWL(0 0 1PS 0 10PS XXXX)
Ijtl2 0 5 PWL(0 0 1PS 0 10PS XXXX)
Ijtl3 0 7 PWL(0 0 1PS 0 10PS XXXX)
Ib 0 13 PWL(0 0 30PS 0 10PS 544uA)
Ix 0 16 PWL(0 0 50PS 0 10PS XXXX)
* Inductance
L1 1 2 2.22PH
L2 1 3 5.556PH
L3 3 4 2.22PH
L4 3 5 5.56PH
L5 5 6 2.22PH
L6 5 7 5.56PH
L7 7 8 2.22PH
L8 7 9 5.56PH
L9 9 10 2.22PH
L10 9 11 2.22PH
L11 12 13 7.56PH
L12 13 14 7.56PH
L13 15 16 2.22PH
L14 16 17 2.22PH
* Junctions
Bg 2 0 jjj0
Ba 4 0 jjj0
Bb 6 0 jjj0
Bc 8 0 jjj0
B1 10 0 jjj0
B2 11 12 jjj0
B3 14 15 jjj0
B4 17 0 jjj0
.model jjj0 jj(rtype=0, rn=1000, icrit=340u, cap=7e-14F)
* Shunt resistance
Rg 2 0 1.176ohm
Ra 4 0 1.1764ohm
Rb 6 0 1.176ohm
Rc 8 0 1.176ohm
R1 10 0 1.176ohm
R2 11 12 1.176ohm
R3 14 15 1.176ohm
R4 17 0 1.176ohm
*Thermal noise added as a current source across resistor
iRjg 2 0 NOISE(43.332232437297748P 0.0P 0.1P)
iRja 4 0 NOISE(43.332232437297748P 0.0P 0.1P)
iRjb 6 0 NOISE(43.332232437297748P 0.0P 0.1P)
iRjc 8 0 NOISE(43.332232437297748P 0.0P 0.1P)
iRj1 10 0 NOISE(43.332232437297748P 0.0P 0.1P)
iRj2 11 12 NOISE(43.332232437297748P 0.0P 0.1P)
iRj3 14 15 NOISE(43.332232437297748P 0.0P 0.1P)
iRj4 17 0 NOISE(43.332232437297748P 0.0P 0.1P)
*Termination
.TRAN 0.1PS 1NS
.file High_tc.txt
.print devv Bg
.print devi Bg
.print phase Bg
```

Script 4.1: J-SIM script that defines the Josephson comparator in Figure 4.3.

Since we are dealing with several biasing sources and the need to minimise dynamic error arising from circuit transients, we found that the best course of action is to stagger the time at which the bias currents are switched on. This is implemented in the first section of the JSIM code. Finally the bias sources of the JTL reach equal values so that I_{JTL1}=I_{JTL2}=I_{JTL3}.

4.3 Initial set-up of J-SIM

Using a modification of the python script used in Section 3.1.1 to generate multiple `.js` files, we began testing our J-SIM simulations by looking at the voltage of the generator junction as a function of the Josephson transmission lines bias currents I_{JTL}.

Frequency and V_{g}: We began running simulations to determine the voltage dependency of J_{g} on input currents at I_{JTL}, by maintaining a constant I_{g} of 520 μA and varying I_{JTL}. V_{g} was averaged in the python script over 1 ns. The results are shown in Figure 4.6 as the current w of V_g against I_{JTL}. An increase in the average DC voltage of J_{g}, in turn translates to an increase in the frequency and the number of SFQ pulses present in a given time frame as shown in Figure 4.7.

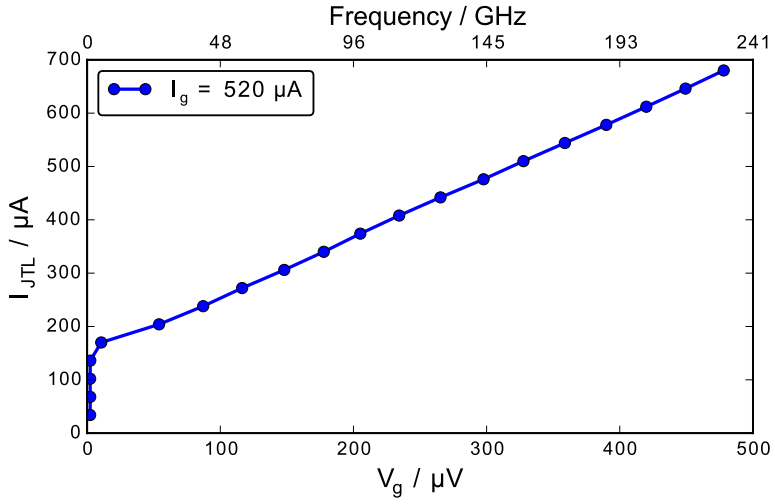


Figure 4.6: Voltage dependency of junction J_{g} against I_{JTL}. I_g represents the input current.

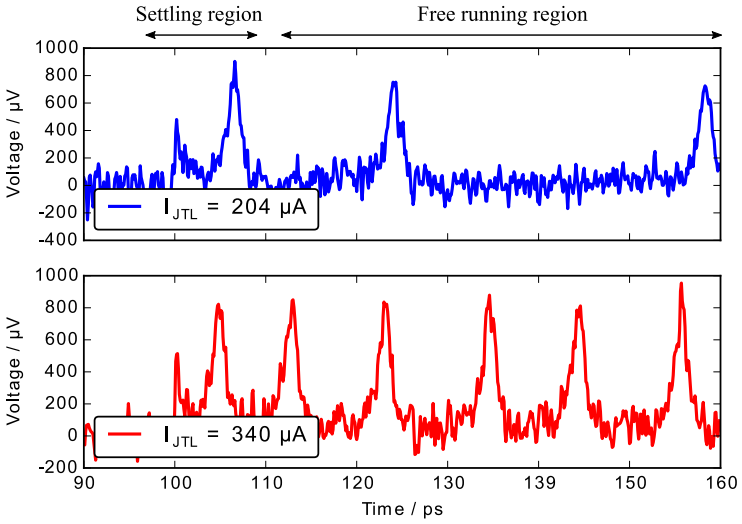


Figure 4.7: Region of time domain JSIM simulations of J_g at biasing values of $I_{JTL} = 204$ and 340 μA respectively. The average voltage of V_g is calculated in the free running region which occurs after the first pulse.

To ensure validity of J-SIM simulations we evaluate the number of flux quanta Φ_0 present in the time domain simulations by integrating the area under $V(t)$ and dividing by Φ_0. As can be seen from Figure 4.8, the number of Φ_0 and SFQ pulses present in the simulation is 23.

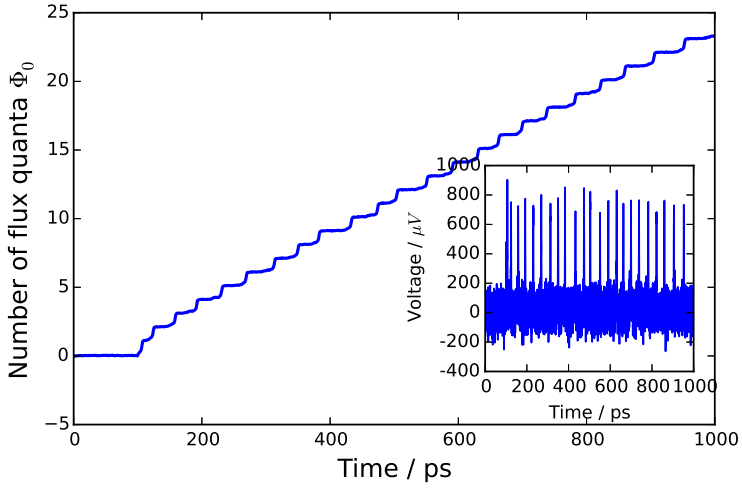


Figure 4.8: Number of Φ_0 over time of the top graph shown in Figure 4.7. Inset shows an expanded plot of voltage over time of generator junction J_g at $I_{JTL} = 204$ μA. Maximum number of Φ_0 equal to number of voltage pulses present in the simulation, both stand at 23 suggesting that the relationship $\int V dt = \Phi_0$ is maintained.

Once confidence in the JSIM simulations was established, we continued testing the expected effect of other sources such as I_{g} and I_{b} on the average voltage output of the generator junction J_{g} due to the way these currents distribute in the structure.

$I_{\mathbf{g}}$ and $I_{\mathbf{b}}$: Again using the same J-SIM Script 4.1, we first looked into the effect of varying both I_{JTL} and I_{g} and the impact that had on the resulting average voltage of J_{g}. We begin first with I_{g} and I_{JTL} shown in Figure 4.9.

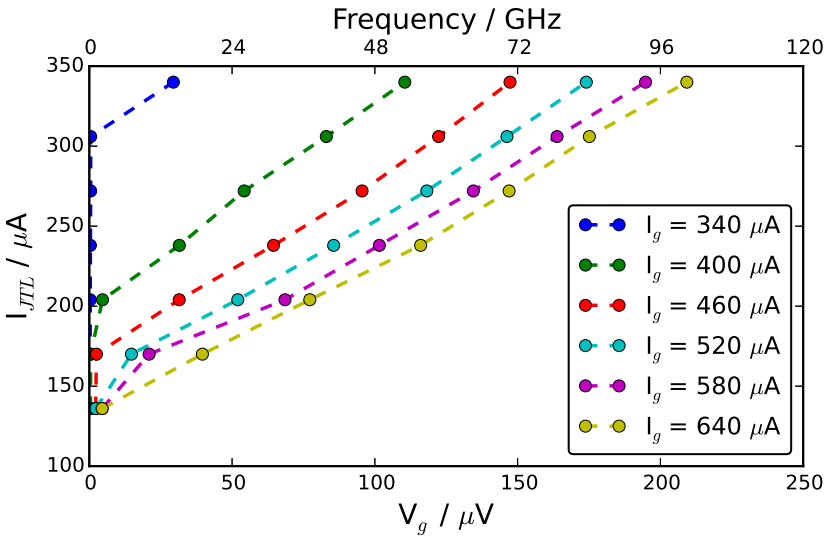


Figure 4.9: Characteristics of average voltage across the generator junction J_g at different values of I_{JTL} and I_g.

Unlike the case when only I_{JTL} is varied, varying both I_{JTL} and I_{g} leads to a series of shifted average voltage output curves of J_{g}. As I_{g} increases the biasing current of I_{JTL} needed for J_{g} to to begin oscillating correspondingly decreases. In the final set of tests, we looked at the effect of varying I_{b} and I_{JTL} on the overall voltage of J_{g}. Similarly to what was done when I_{g} was varied, we modified our python programme to cycle through several values of I_{b}, resulting again in a series of shifts in the average voltage curves as is shown in Figure 4.10. These shifts in both Figures 4.9 and 4.10 are a result of superposition of bias currents leading to an increasing contribution in the total current through J_g. Changes in I_{g} cause a bigger shift since it is directly connected to the generator junction as opposed to I_{b}

which is much further away in inductance terms and has minimal influence on J_g.

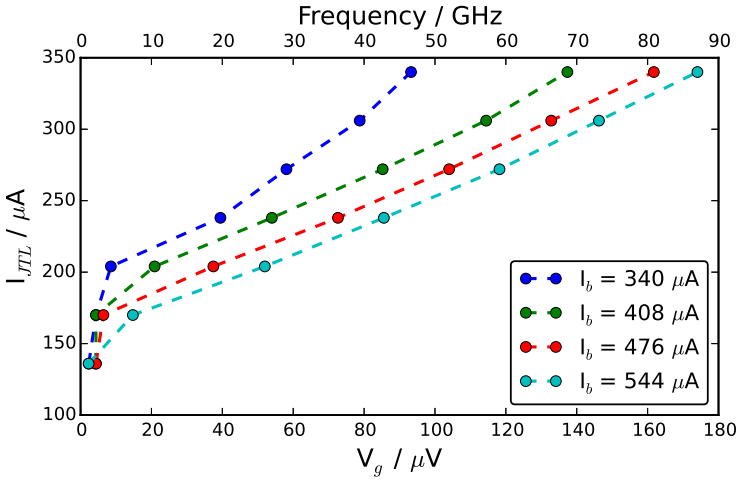


Figure 4.10: I-V graphs of Comparator and generator junctions at different bias values of I_b and I_JTL whilst I_g is maintained at 520 μA.

The average voltages across the generator and comparator junctions J_g, J_3 and J_4 at different values of I_b are shown in Figure 4.11. It can be seen that the cleanest grey zone edge is obtained for $I_\mathrm{b} = 544\mu$A (which is the value used by Ozele *et al.*).

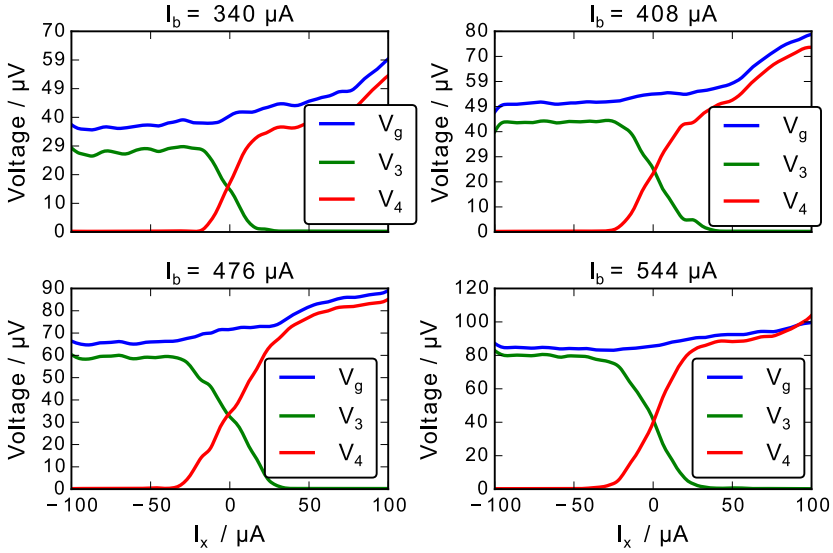


Figure 4.11: Average voltage across comparator and generator junctions at different bias values of I_b, I_g and I_JTL are maintained at 520 μA and 238 μA. Values of I_b other than 544 μA result in some feature/steps in the grey zone edge, suggesting either unbalance in the comparator, or storage of flux in the comparator loop.

4.4 Comparison of J-SIM simulations to Oelze *et al.* data

To ensure validity of the J-SIM model, we compared our simulation results to the measurements of Oelze *et al.*[1]. We first begin by comparing the the IV graphs obtained by the group to our J-SIM output. As mentioned in Section 2.2.3, Oelze *et al.* showed the average voltage dependence of junctions J_g, J_3 and J_4 on the signal current I_x at $T = 40\ K$, the results of which are shown in Figure 4.12. It can immediately be seen that both I-V graphs from Oelze *et al.* and J-SIM exhibit similar key characteristics i.e. self oscillation of Junctions J_3 and J_4 at high values of the signal current I_x leading to the observed branches on the left and right sides of Figure 4.12.

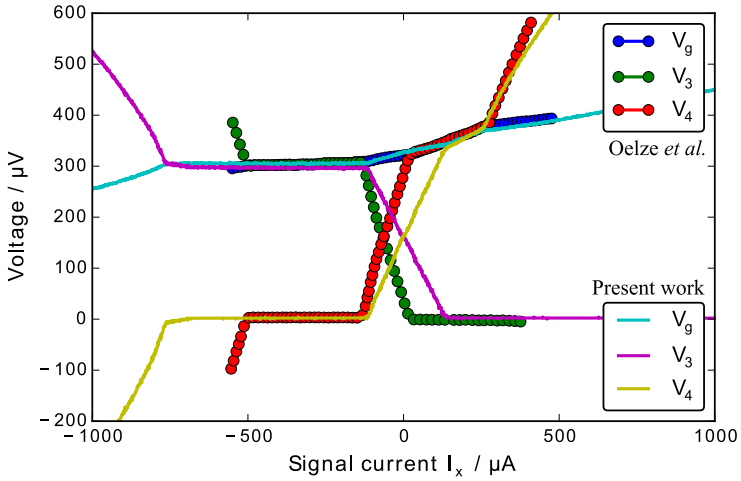


Figure 4.12: JSIM output of the generator and comparator junctions and the experimental results obtained by Oelze *et al.* at biasing values of $I_g = 520\ \mu A$ and $I_{JTL} = 340\ \mu A$. Data adapted from Oelze *et al.* [23]

The key difference in the two sets of results lies within the grey zone width. In both the J-SIM output and the measurements obtained by Oelze *et al.* junction J_4

[1]In addition to experimental measurements Oelze *et al.* performed simulations using PSCAN but did not publish details of their model we therefore focus on their experimental measurements

begins to transition from a no switching state at an approximately similar signal current I_x values. However once the voltage of both junctions starts to rise they end at two different points. Comparing the switching probability of the data from Oelze *et al.* and the J-SIM output in Figure 4.13 best illustrates this.

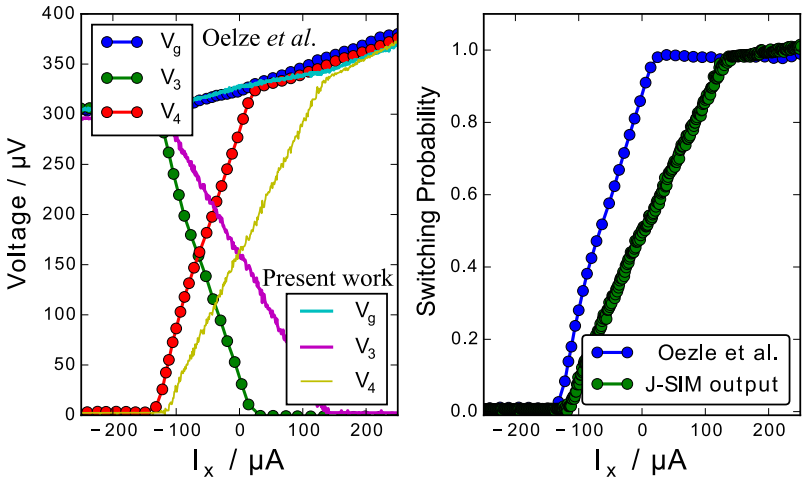


Figure 4.13: A close up of the transition region of Figure 4.12 and the resulting switching probability ($p = V_4/V_g$) graph. The grey zone ΔI_x for both Oelze *et al.* and J-SIM stand at 113 μA and 209 μA respectively. Data adapted from Oelze *et al.* [23].

Comparing the switching probability of the J-SIM output (V_4/V_g) to that of the data collected by Oezle *et al.* shows the transition between the two data sets from a switching probability of "0" to "1" start at approximately equal signal currents but end at different points. This translates into two different grey zones which stand at 113 and 209 μA respectively. The discrepancy between the two widths is most likely attributed to the way in which the JSIM model is set-up. Actual devices suffer from fabrication variations in parameters resulting in a spread of critical current of the junctions, so instead of a single I_c value for all Josephson junctions as was assumed in the J-SIM model, the real device likely has a critical current I_c spread of $\pm 15\%$ as reported by Oelze *et al.*. This spread in critical current translates into a discrepancy between the recorded grey zone width from JSIM and that from the data presented by Oelze *et al.* This will be consider parameter spreads are

introduced into simulations in Chapter 5. This discrepancy is only significant at high voltages, on the other hand at lower voltage values of J_g the error is much less prominent as shown in Figure 4.14.

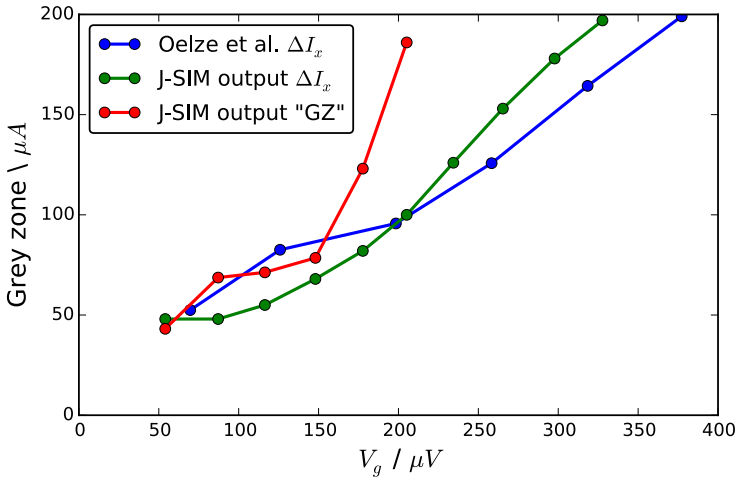


Figure 4.14: Graph showing the comparison of the different grey zones from both JSIM (green and red) and the experimental data collected by Oelze *et al.* Data adapted from Oelze *et al.* [23].

Using the definition of the grey zone described in Section 4.1, again we compared the grey zone recorded by Oelze *et al.* to the J-SIM output at lower average voltage values for J_g. From Figure 4.14 it can be seen that the grey zone of the J-SIM output as defined by Haddad *et al.* and labelled GZ is a good approximation to that recorded by Oelze *et al.* but starts to diverge substantially above 150 μV which is most likely due to the fact that the switching curves are poorly represented by a single error function due to the presence of a small plateau in the middle curve meaning that the gradient at switching probability $p = 0.5$ does not represent the grey zone but instead the steepness of the plateau. The grey zone as defined by ΔI_x is a much closer estimation to the experimental data at higher V_g values.

The ability of JSIM to produce IV characteristics of the Josephson comparator that are very similar to those from the experimental data obtained by Oelze *et al.* makes it a very powerful simulation tool with a tolerable discrepancy for our

simulations. In the next section we take a further step in analysing the Josephson comparator by investigating the effect of the biasing on grey zone width and the decision process manifested as the switching time of junctions J_3 and J_4 in particular.

4.5 Further testing and simulation results

I_{JTL} and grey zone width: In the following section we utilise J-SIM to further test the effect of the biasing current of the Josephson comparator at different I_{JTL} values. Using the definitions of the grey zone width stated in Section 4.1 we perform simulations and collect the resultant grey zone as shown in Figure 4.15.

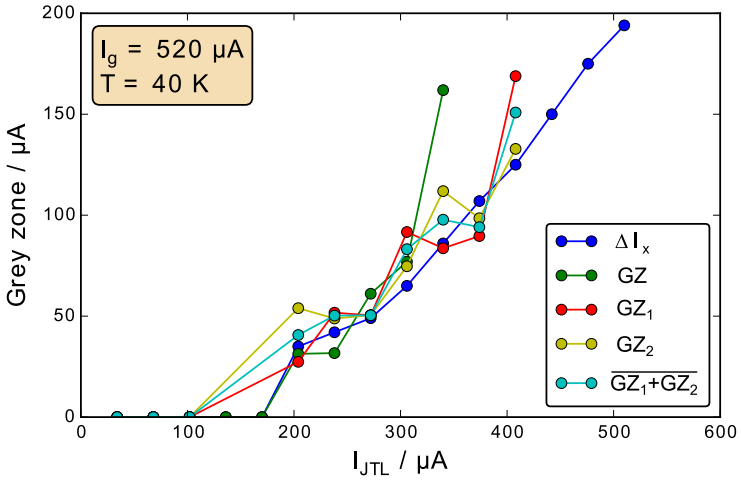


Figure 4.15: Graph illustrating all the different definitions of the grey zone vs $\mathrm{I_{JTL}}$ at $\mathrm{I_g} = 520\ \mu A$, $T = 40$ K. Both the grey zone for $\mathrm{GZ_1}$ and $\mathrm{GZ_2}$ are shown and the average of both is also plotted as $\overline{\mathrm{GZ_1} + \mathrm{GZ_2}}$

Figure 4.15 shows above a threshold where I_{c} is exceeded, the grey zone has an approximately linear dependancy on I_{JTL}. The variation between the different methods of defining the grey zone as described in Section 4.1 is quite interesting. Whilst all methods display similar characteristics i.e. a linear relation between grey zone and I_{JTL}, the grey zone calculated using the gradient method for one or two steps and given as GZ, $\mathrm{GZ_1}$ and $\mathrm{GZ_2}$ is a good approximation of ΔI_{x} at certain values but starts to diverge at higher bias currents, i.e. at lower values of I_{JTL},

GZ_1, GZ_2 and $\overline{GZ_1 + GZ_2}$ are in good agreement. This is not the case as the value of I_{JTL} increases i.e. at $I_{\mathrm{JTL}} > 340\ \mu A$. This can be explained via the switching graphs where the ERF error function from Equations 4.2 and 4.3 are a poor fit as shown in Figures 4.16 and 4.17.

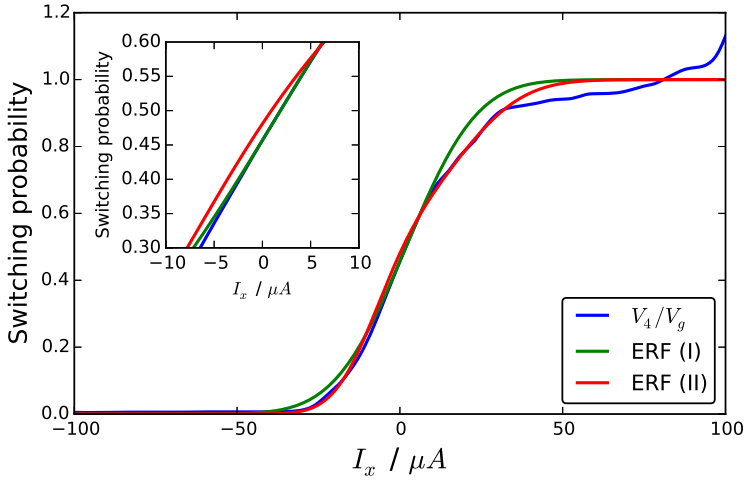


Figure 4.16: The switching curves of the comparator junction J_4 at frequency of 25 GHz at $I_{\mathrm{g}} = 520\ \mu A$ and $I_{\mathrm{JTL}} = 204\ \mu A$.

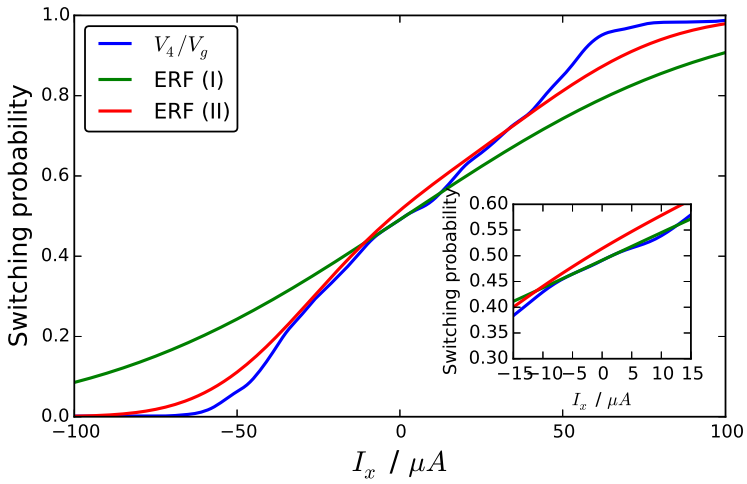


Figure 4.17: The switching curves of the comparator junction J_4 at frequency of 100 GHz at $I_{\mathrm{g}} = 520\ \mu A$ and $I_{\mathrm{JTL}} = 374\ \mu A$.

At higher current biasing of I_{JTL} results in a plateau which in turn effects the grey zone approximations using GZ, GZ_1 and GZ_2. Therefore for the reminder of

this report ΔI_{x} will act as the reference grey zone width which other approximations are compared to.

Decision and switching time: Investigations of the decision process of the Josephson comparator can be visualised through averaging of the switching time of the device. In order to do this we first begin by running multiple simulations of a single J-SIM script and collecting the time difference between the time for the first voltage peaks of V_{g} and V_3 or V_4. An example of this is shown in Figure 4.18 where 300 JSIM simulations at a signal current $I_{\mathrm{x}} = 0$ μA were run. Each measurement includes a $\approx$ 35 ps delay which is the time for a signal to travel across the JTL. The additional switching time is then set by the effect of noise in the comparator loop.

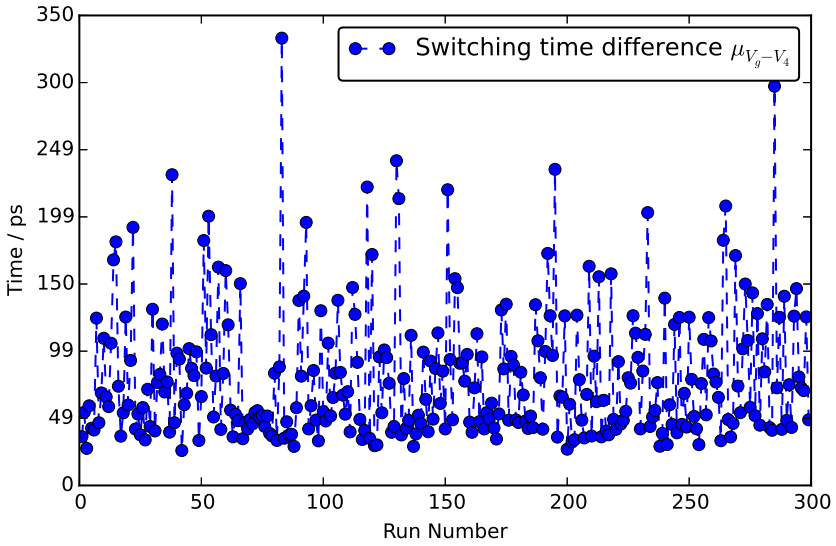


Figure 4.18: Switching of the Josephson comparator with respect to the generator junction using the circuit parameters provided by Oelze *et al.* at $T = 40$ K with $\mathrm{I_{JTL}}$=204 μA at $\mathrm{I_x}$=0 μA.

The nature of Josephson junctions and the way in which noise is added to J-SIM simulations ensures that no two runs are the same. By taking the mean switching of the time difference for the simulations performed over a wide range of signal currents I_{x}, we can plot the switching time dependence of the comparator on the

input signal I_{x} as shown in Figure 4.19. For J_3, the mean switching evolves as I_{x} increases from negative values reaching a peak value before decreasing at large positive values.

The region shown in Figure 4.19 corresponds to the grey zone switching region of J_3 and J_4. At large positive values of I_{x}, the arrival of a flux quantum in the comparator loop is sufficient to always switch J_4, so the time delay is therefore set by I_{JTL}. For smaller/negative values of I_{x} there is an extra delay until a random noise fluctuation helps switch it.

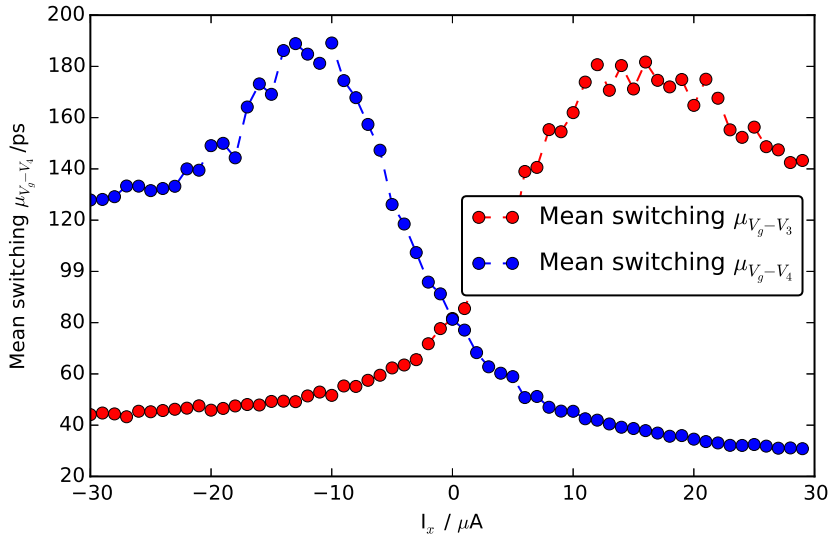


Figure 4.19: The average mean switching time of J_3 and J_4 at I_{JTL}=204 μA with respect to J_g.

This transition is indicative of the switching of the Josephson comparator and can be related directly to its decision making process. By plotting the dependence of the mean switching at different values of I_{JTL} over the same signal current I_{x} as shown in Figure 4.20, we see the effect of increasing the voltage of J_{g} and in turn the number of SFQ pulses in the circuit on the decision process in the comparator.

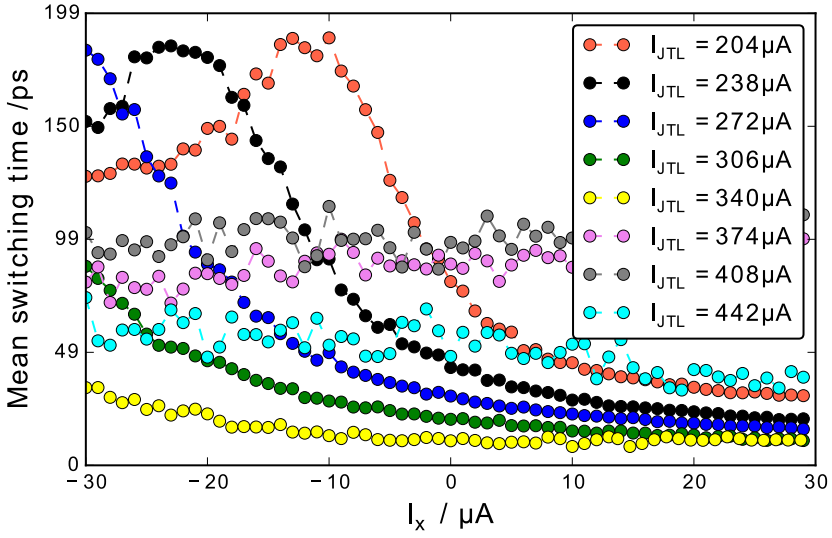


Figure 4.20: Mean switching time of J_4 at different values of $\mathrm{I_{JTL}}$.

At lower biasing values of I_{JTL} the mean switching of junctions J_4 climbs to a maximum value as a function of I_{x} before beginning to descend and vis-versa for junction J_3, this behaviour is absent in higher values of I_{JTL} where the mean decision time is almost constant[2], considering only the maximum values of the mean switching against values of I_{JTL} at $204 - 272$ μA shows that at low values of I_{JTL} the mean switching of the device stays around ≈ 190 ps. At large positive values of I_{x} the switching time achieves low values. There is also a dependancy of the switching time on I_{JTL} due to the biasing of I_{JTL} affecting the current through the generator junction and thus the frequency of single flux quantum generation.

We can relate these observations back to Figure 4.16 showing the smallest grey zone recorded at $I_{\mathrm{JTL}} = 204$ μA, where the mean switching time varies considerably over the grey zone. An ideal comparator would have the smallest mean switching time variation and the smallest possible grey zone. However this unattainable, instead the smallest grey zone width corresponds to a large variation in the mean switching time, therefore operation of a Josephson comparator requires a sacrifice

[2]This is problematic to determine with absolute certainty due to the narrow range of I_{x}.

between either fast operation where the variation in mean switching time is minimal but resulting in a large grey zone, or a narrower grey zone width with a slower device.

Variations in inductances: In addition to the biasing of the comparator we looked at the effect of altering the inductance distribution on overall grey zone width. By maintaining an overall inductance of the loops similar to that reported by Oelze *et al.* we used the flexibility of J-SIM to alter the way in which the inductances of the JTL loops were distributed resulting in four different possibilities that still hold true to the relationship between the inductors described in Section 4.2.1. In addition to this we also varied the inductance values of L_{11} and L_{12} to look into the effect on grey zone width of altering the distribution of I_b to increase the bias current to J_3 and J_4. Figure 4.21 shows the grouping of the different inductors in the circuit whilst both Table 4.1 and Figure 4.22 summarises the systems investigated and the grey zone widths recorded.

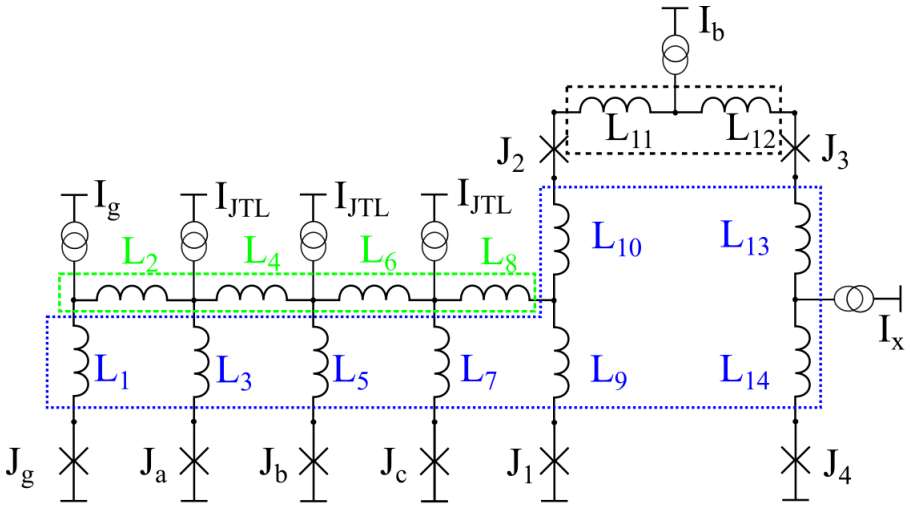


Figure 4.21: Circuit schematic of the inductance distributions that will be used in the JSIM simulations. By defining the inductances we shall use as L_1=L_3=L_5=L_7=L_9=L_{10}=L_{13}=L_{14} and L_2=L_4,=L_6,=L_8, allows us to manipulate the current distributions from I_b in the large comparator loop and observe the resultant effect on grey zone width which is reproted in Table 4.1 for all grey zone and in Figure 4.22 for ΔI_x.

System Label	Inductor and inductance values / pH				Lowest J_g voltage and grey zone recorded						
	L_1	L_2	L_{11}	L_{12}	V_g / μV	ΔI_x/ μA	V_g / μV	GZ/ μA	V_g / μV	GZ_1 / μA	GZ_2 / μA
a	1	7	9	9	50	36	50	26	50	40	45
			10	8	93	48	93	53	93	36	69
			11	7	52	57	92	82	52	54	75
			12	6	50	49	50	80	50	54	31
			13	5	54	32	54	26	54	27	51
			14	4	50	53	50	38	50	40	56
			15	3	48	54	92	95	48	53	52
			16	2	46	41	46	61	46	55	31
			17	1	89	39	52	28	52	34	43
			18	0	92	52	52	53	52	39	61
b	2	5	7	7	50	35	50	31	50	28	53
			8	6	83	48	50	43	83	46	58
			9	5	57	53	84	93	116	52	58
			10	4	50	39	50	37	50	56	39
			11	3	48	29	48	22	85	40	50
			12	2	88	48	54	43	54	56	52
			13	1	87	56	52	57	52	54	47
			14	0	50	41	50	36	87	76	36
c	3	3	5	5	48	32	48	21	74	35	35
			6	4	75	46	46	36	75	37	52
			7	3	46	49	46	50	77	40	52
			8	2	44	34	44	26	78	56	36
			9	1	48	30	48	30	48	31	34
			10	0	77	48	48	33	48	55	67
d	4	1	3	3	75	32	5	27	43	25	26
			4	2	35	47	5	36	77	44	90
			5	1	40	48	40	64	40	43	39
			6	0	33	28	25	18	25	32	48

Table 4.1: List of all the configurations tested to investigate the effect of inductance distribution using J-SIM. Total inductance of system maintained at 10 pH and 24 pH for the JTL and comparator loops respectively L_1=L_3=L_5=L_7=L_9=L_{10}=L_{13}=L_{14}, L_2=L_4=L_6=L_8. The device is biased at I_g=520 μA whilst the corresponding I_{JTL} tends to be the lowest value at which the device starts oscillating which is 204 μA for most, whilst for some inductance distributions that value shifts to 238 μA. This is shown in Figure 4.22.

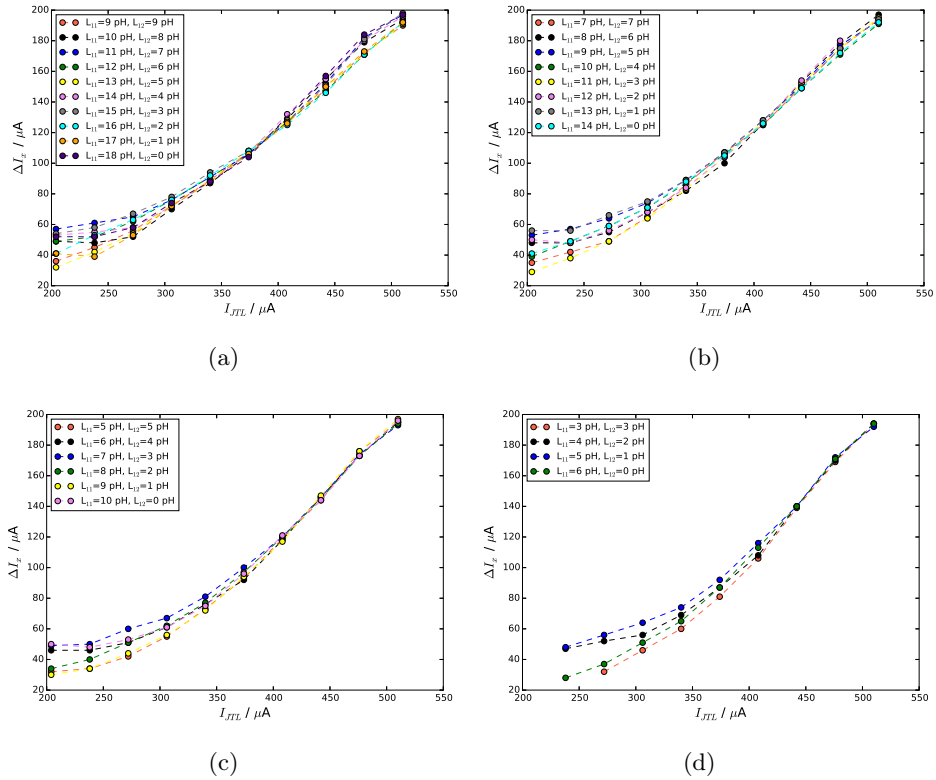


Figure 4.22: Graphs of the collected grey zone widths ΔI_x at I_g=520 μA for different inductance distributions in the JTL and the comparator.

Current redistributions through changing the ratio of L_{11} to L_{13} has most of its impact at lower frequencies as shown in Figure 4.22. As the frequency increases the grey zone width converges into almost a single curve for systems (c) and (d), whilst the grey zone widths for systems (a) and (b) cross at $I_{\mathrm{JTL}} = 374$ μA and 442 μA respectively. The sensitivity of the comparator to current redistribution is of quite interest since it allows us the ability to fine tune the performance of the comparator not only by manipulating the magnitude of the bias currents but also through varying the dimensions and shape of the comparator loop, some thing that would be more difficult in the high T_{c} material used by Oelze *et al.* due to restrictions on junction placement. In general though the best performance is obtained for a balanced comparator loop with $L_{11} = L_{12}$, keeping the comparator loop and the connection symmetric is therefore desirable in fabrication.

4.6 Summary

In this chapter we have outlined the evaluations criteria on which to evaluate a Josephson comparator circuit either as a single step grey zone or that with a plateau described by Equations 4.2 and 4.3. We have also outlined the initial comparator setup in JSIM shown in Script 4.1. By comparing JSIM output to that of a device fabricated by Oelze *et al.* [23] in a high T_c substrate gives encouragement as to the validity of the JSIM model, as shown in Figure 4.12 similarities in key features between the graphs, such as the presence of negative voltage and the self oscillation of junctions on both sides of each graph. The variations in the recorded grey zone between the two graphs can be attributed by the absence of a critical current spread in the JSIM model which is present in the work by Oelze *et al.* [23], this is investigated in the following chapter. where by utilising JSIM we investigate the effect of adding critical current spreads to the overall performance of the Josephson comparator.

Chapter 5

Simulations testing the feasibility of using low T_c nanobridge weak links in Josephson comparators

5.1 Introduction

The use of nanobridge weak links as the active Josephson element in an RSFQ circuit and in particular Josephson comparators introduces high degrees of flexibility in fabricating and testing the circuits in labs without the need of to rely on integrated tunnel junction technology that can only be fabricated from predetermined cell libraries by specialised foundries such as Hypres Inc, whilst nanobridge weak links are much easier to produce for labs with nanoscale fabrication facilities with the only limiting factors being either resist resolution in lift off and RIE systems, or thin film poisoning in FIB. Both of these limiting factors can be overcome by iteration i.e. optimisation of EBL process can allow lift-off and RIE processes the can obtain nanobridge weak links with dimensions comparable to the coherence length ξ_{GL}, whilst a recently developed Ne/He FIB system might be capable of overcoming the film poisoning issue that surrounds Ga/FIB. In the following chapter we shall perform JSIM simulations of the Josephson comparator designed by Oelze *et al.* but

with the high T_c parameters replaced by those appropriate to low T_c nanobridges. We then report report on operational performance and limits of the circuit. We begin by investigating the range operational parameters likely for a circuit based on low T_c thin films.

I_c and the Operating temperature: As the most studied material used in low T_c devices, niobium will be the focus of this thesis as the material of choice in simulations. Nb films can be obtained via either e-beam evaporation or sputtering with a maximum T_c of 9.25 K. The T_c depends on factors such as the base pressure of the deposition system and the processing of the nanobridge. With such a high T_c relative to other low temperature materials such as aluminium and titanium, it is a very convenient material to test in liquid helium and as such will be the remaining focus of simulations in this chapter. We begin by calculating the likely temperature dependence of the critical current. We assume a Nb nanobridge behaves as a dirty metal weak link and apply the KO(I) theory using Equation 1.55 for a typical normal resistance R_N of 1 Ω and taking into account the range of T_c obtained due to the choice of fabrication method [108, 113]. The expected critical current variation is shown in Figure 5.1.

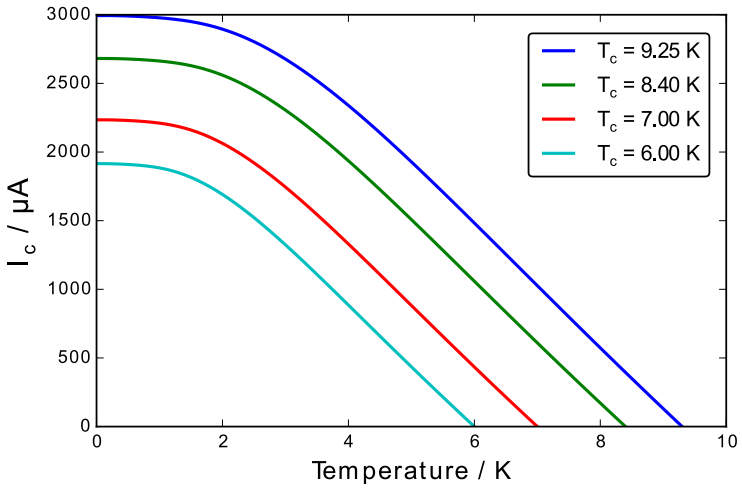


Figure 5.1: Temperature dependence of the critical current I_c calculated from the KO(I) theory in Equation 1.55. The choice of T_c reflects the possible transition temperatures obtained due to the choice of fabrication methods.

In order to successfully operate an RSFQ circuit the active Josephson element must be overdamped where $\beta_c \ll 1$. For devices based on tunnel junctions β_c is usually greater than unity due to high capacitance. We can calculate the capacitance per unit width between the banks of the nanobridge weak link using [115]:

$$C = \epsilon_0 \epsilon_r \frac{K(\kappa')}{K(\kappa)} \tag{5.1}$$

where ϵ_0 is the vacuum permittivity, ϵ_r is the average relative permittivity of the nanobridge region between the banks, K is the elliptic integral of the first kind, κ is the modulus which depends on the dimensions of they gap between the electrodes, κ' is its complementary modulus. Taking a value of $\epsilon_r \approx 2.4$[1] for the nanobridge region between banks of 1 μm in width, gives an estimated capacitance of $\approx 2.5 \times 10^{-17}$F. Inputting this value in the Stewart-McCumber from the RCSJ model for a junction with $R_N = 1\ \Omega$ and $I_c = 800\ \mu A$ at $T = 8$ K calculated from Figure 5.1 for a device with $T_c = 9.25$ K results in $\beta_c = 2\pi I_c R_N^2/\Phi_0 = 6 \times 10^{-5}$ which falls well within the limit $\beta_c \ll 1$, suggesting that unlike tunnel junctions there will be no hysteresis related to the capacitance. However many nanobridges are found to have hysteretic IV characteristics.

In 1974 Skocpol *et al.* [117] introduced a widely accepted explanation for the origin of this hysteresis. They proposed that when the applied bias exceeds the critical current of the nanobridge, Joule heating in the nanobridge results in a hot spot formation which in turn results in the nanobridge region entering the normal state. the current needed to self sustain this normal hotspot region is lower than the critical current. This in turn leads the current voltage characteristics of the overdamped weak link to resemble that of a hysteretic underdamped junction, resulting in the need to reduce the applied bias to well below I_c to get back into the superconducting state. This return current value is referred to as the re-trapping

[1]Since half the nanobridge region is made approximately comprised of air where $\epsilon_{r,\ air} \approx 1$ and SiO_2 where $\epsilon_{r,\ SiO_2} = 3.9$ [116], 2.4 is a good approximation to take for $\epsilon_{r,\ nanobridge}$.

current I_r and is a function of the geometry, materials and operating temperature of the nanobridge and banks. The hotspot extends into the banks over a thermal length scale η defined as $\eta = \sqrt{\kappa t/\alpha}$ where κ is the thermal conductivity, α is the heat transfer coefficient to the substrate and t is the thickness of the film. Skocpol, Beasley and Tinkham (SBT) modelled I_r for nanobridge weak links where the dimensions of the structure are short compared to this thermal length scale as:

$$I_r \approx \sqrt{\left(\frac{\kappa t^2 T_c}{R_N}\right)\left(1 - \frac{T}{T_c}\right)} \tag{5.2}$$

Plotting the temperature dependence of I_c and I_r for a nanobridge with dimensions $(l \times w \times t)$ of $(100 \times 80 \times 120)$ nm, $R_N = 1\ \Omega$ and $T_c = 9.25$ K results in a plot describing the possible operating temperatures of a nanobridge where the current voltage characteristics of the weak link are non-hysteretic as shown in Figure 5.2.This shows that the possible operating temperature for a non-hysteretic nanobridge weak links extends to about 2 K below T_c.

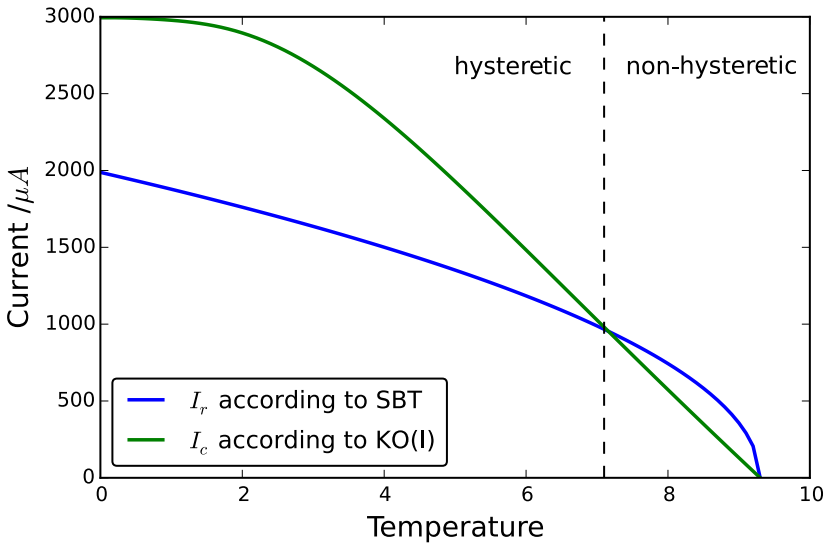


Figure 5.2: Predicted temperature dependence of the critical current I_c and the re-trapping current I_r of a typical Nb nanobridge based on the KO(I) theory and the SBT model of Skocpol *et al.*

Repeating the calculation for Nb films of different critical temperatures results

in a similar set of curves as shown in Figure 5.3.

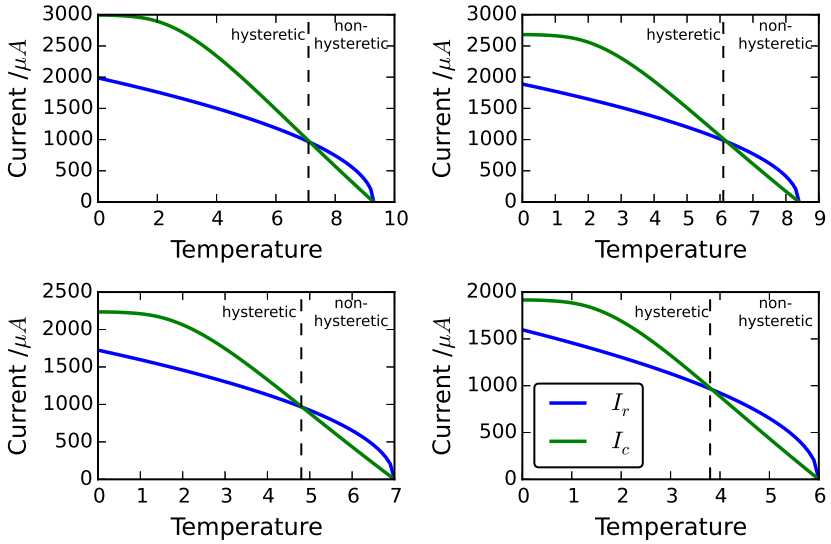


Figure 5.3: Temperature dependence of the critical current I_c and the re-trapping current I_r based on the KO(I) theory and the SBT model at different critical temperatures T_c.

The relatively high T_c of niobium leads to a very high critical current density as $T \to 0$. For this reason, we can see from Figure 5.3 that the non-hysteretic region generally has critical currents from zero to about 1 mA. In practice we might want to avoid being to close to T_c or to the hysteretic region so critical currents of several hundred microamps are likely.

Noise at low T_c: Using for the moment the circuit parameters of the Josephson comparator described in Section 4.2, we look into the effect of adding noise at temperatures close to T_c for a lower operating temperature. For instance, assuming $R_N = 1\ \Omega$ we can estimate the corresponding temperature as is shown in Figure 5.4 where the $I_c = 340\ \mu$A. Maintaining the total loop inductances as 10 pH and 24 pH for the JTL and comparator loops respectively and adding noise at $T = 5.1$ K and 8.4 K as is shown in Figure 5.5, we see little difference between the two simulations suggesting that at low temperatures small differences in the noise temperature have little influence on overall device performance as we might expect.

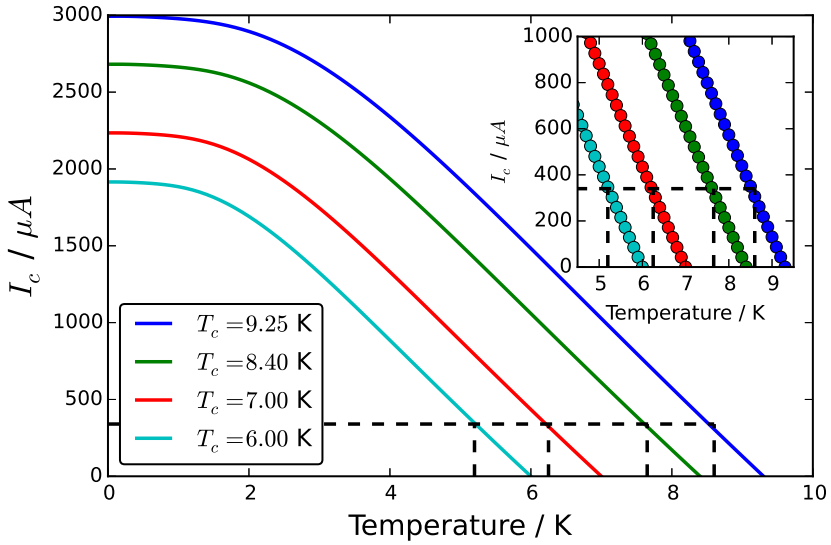


Figure 5.4: Temperature dependence of the critical current for low T_c Nb nanobridge at different T_cs. The dashed line represents the corresponding temperatures at which $I_c = 340\ \mu A$.

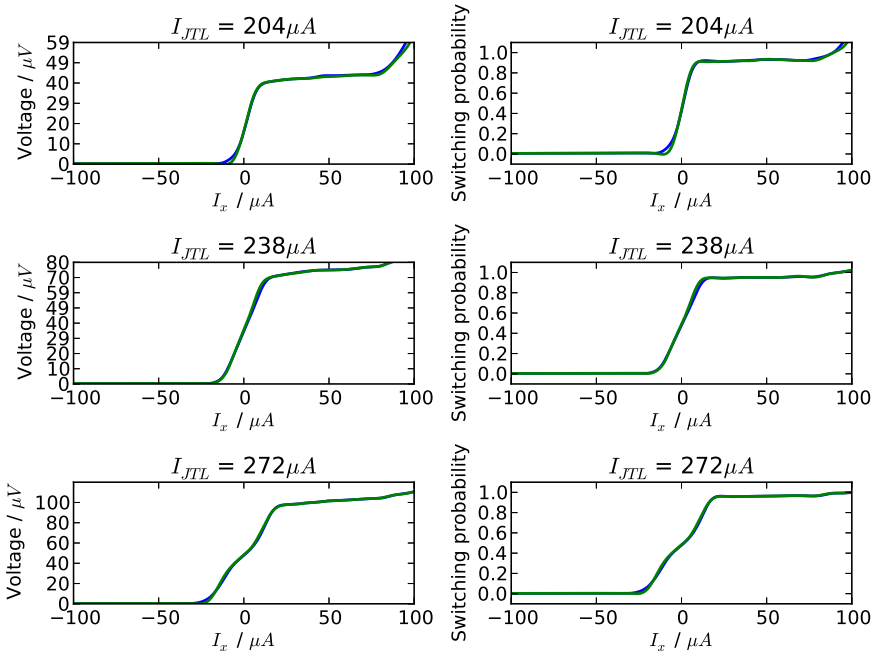


Figure 5.5: Blue and green lines on each plot represent switching of J_4 for noise added at $T = 8.4$ K and 5.1 K respectively, with $I_c = 340\ \mu A$ at different I_{JTL} values and I_g maintained at 520 μA.

Loop inductance: In addition to the temperature dependant re-trapping current, the total loop inductance of the Josephson comparator places further restriction on the operating temperature of the Josephson comparator. Optimal operation of the Josephson comparator requires that the value of the screening parameter β_L is equal to or as close as possible to 1 to ensure that the loops are not in the flux storing state. Taking β_L as:

$$\beta_{\mathrm{L}} = \frac{2LI_{\mathrm{c}}(T)}{\Phi_0} \tag{5.3}$$

we can plot the dependence of the total loop inductance on the critical current (and in turn the temperature) as shown in Figure 5.6.

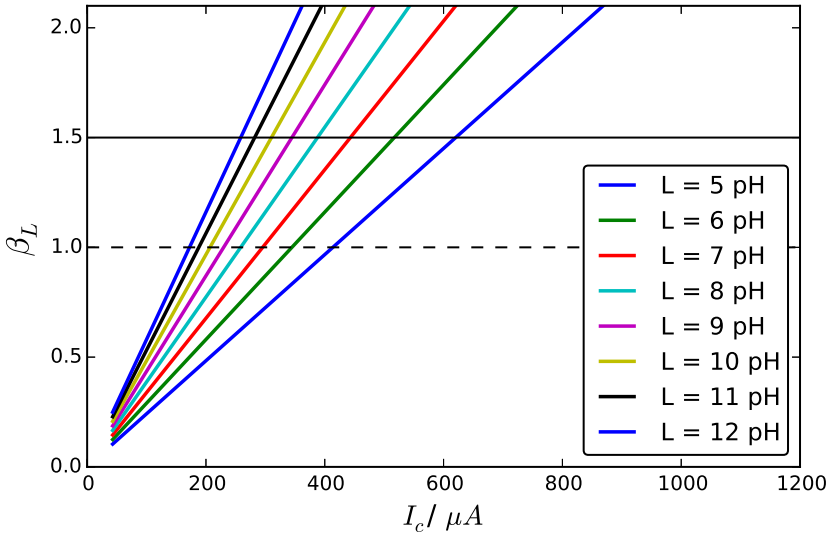


Figure 5.6: The critical current dependence of β_L as a function of total loop inductance for $T_{\mathrm{c}} = 9.25$ K. For optimal operation of the Josephson comparator, we restrict ourselves to choosing a total loop inductance so $\beta_L \approx 1$. This in turn places a restriction on the possible critical currents and in turn the temperatures that can be used. The solid black line represents the β_{L} that was used by Oelze *et al.* in their high T_{c} device.

Based on the assumption from 3D-MLSI simulations that the total inductance of a Nb track is of order 1 pH per μm, and the limitations of actual loops that can be fabricated, we have decided to choose a total loop inductance of 7 pH and

12 pH for the JTL and comparator loops respectively. Although smaller inductance loops can probably be fabricated by EBL, making the structures too small would make it harder to extract heat to avoid hysteresis. We used these inductances in combination with a normal resistance of $R_N = 1\ \Omega$, I_c calculated using the KO(I) theory for Nb, and with a critical temperature of $T_c = 9.25$ K so as to allow for the highest possible I_c within the constraints of $\beta_L = 1$.

5.2 Operating parameters and process variation in simulations

In order to gain a clear picture of the performance of the Josephson comparator and build a more realistic model of the device we introduced critical current spreads to our JSIM models. In a real device these spreads would be a result of variation in the nanobridge dimensions that arise due to the tolerance of the fabrication process.

Introducing variation: Changes in the length and the width of the nanobridge translate directly to variations in the recorded critical current. Using the a random number generator from the python scientific library *Numpy* with a Gaussian distribution, we recreate this spread in critical current where the mean of the distribution is the recorded I_c obtained from the KO(I) theory and the upper and lower limits are the percentage I_c spreads, an illustration of this is shown in Figure 5.7.

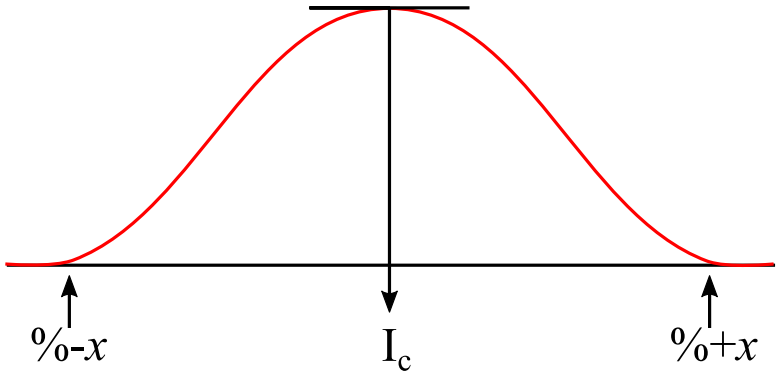


Figure 5.7: Illustrative representation of the *Numpy* random distribution in I_c used to mimic the critical current spreads in nanobridges. x represents the percentage spread and the mean is that of the average critical current according to the KO (I) theory.

5.3 Simulations with variations in I_c

Critical current spreads due to variations in the length of the nanobridge weak links are first investigated. We assume that a small variation in length results in a very small linear variation in the value of the normal state resistance R_N so that it can be taken as approximately constant. In contrast we assume that I_c wil tend to depend exponentially on the length of the bridge and will tend to vary more rapidly than R_N. The variations in I_c will in turn vary the I_cR_N product of the junction. Using the python script described earlier, we randomly assigned critical currents to all the different junctions and recorded the resultant average voltage of the generator and comparator junctions. Utilising the KO(I) theory we performed simulations for a Nb nanobridge weak link of dimensions ($l \times w \times t$) of ($100 \times 80 \times 120$) nm and a normal state resistance $R_N = 1\ \Omega$, taking into account the restrictions placed on operating temperature due to hysteresis as a result of thermal heating and our choice of total inductances of the JTL and comparator loops. Simulations were performed at $T = 9,\ 8.5,\ 8$ and 7.5 K for a device with an assumed transition temperature of $T_c = 9.25$ K. The choice of transition temperature allows simulations of a broad range of critical currents within the confines of operational limits and whilst maintaining a biasing value of I_g of $1.6I_c$. Figure 5.8 shows the set-up of the comparator and the junctions with random assignments of I_c.

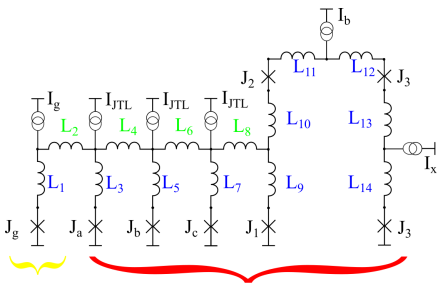


Figure 5.8: illustration of the inductances to be used in JSIM simulations in addition to critical current distribution in device. The generator junction J_g uses the mean value of the Gaussian distribution representing the calculated I_c from the KO(I) theory, the junctions highlighted by the red bracket use the randomly assigned critical current values extracted from the Gaussian distribution. I_g is maintained at $1.6I_c$.

The first set of simulations were to establish the ideal operating parameters of the comparator. In a similar manner to Oelze *et al.* we began by establishing the biasing values of I_{b} that result in the highest average voltage of the generator junction J_{g} at the lowest biasing value for I_{JTL} and $\pm 5\%$ critical current spread. The results are shown in Figure 5.9.

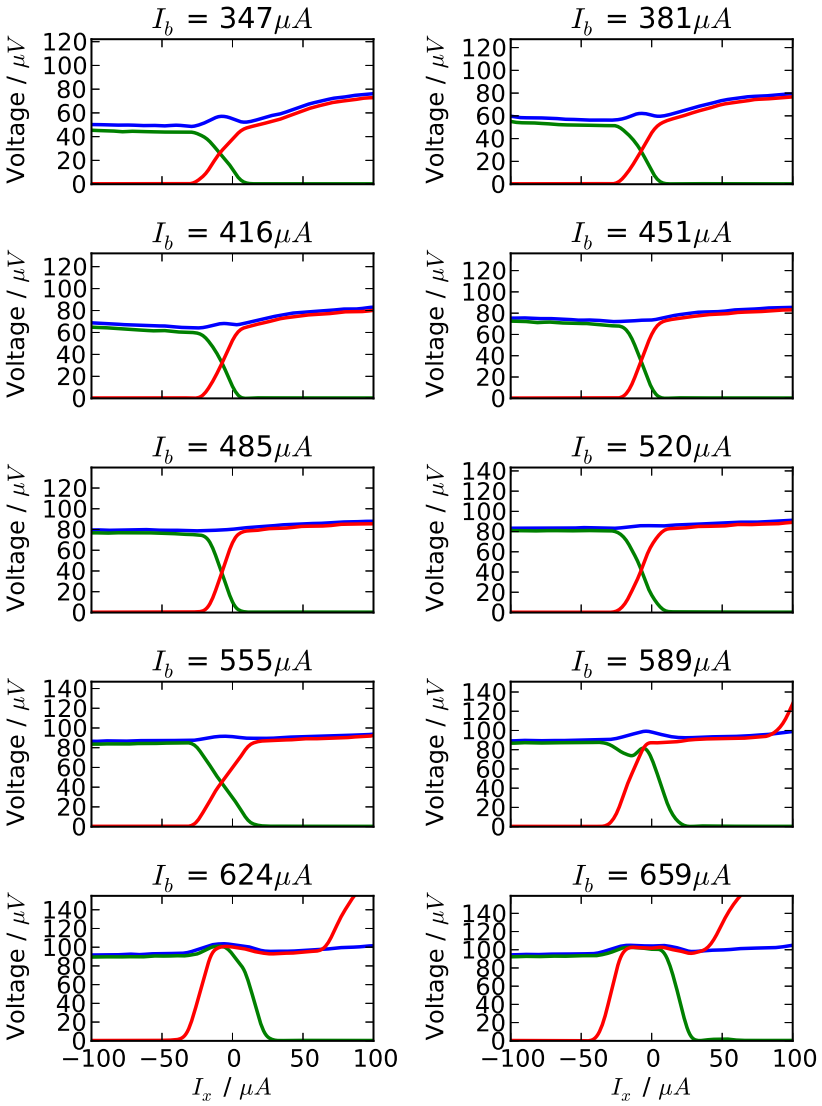


Figure 5.9: Current voltage characteristics of the Josephson comparator for junctions J_{g} (blue), J_3 (green) and J_4 (red) respectively, at different biasing values of I_{b} where current sources I_{g} and I_{JTL} are maintained at $1.6I_{\mathrm{c}}$ and $0.5I_{\mathrm{c}}$ respectively. The curves are for a $\pm 5\%$ critical current variation.

The output average voltage of the generator and comparator junctions is not affected by the biasing value of I_{b} up to and including a value of $I_{\mathrm{b}} = 1.6I_{\mathrm{c}}$, at which point the shape of the resulting switching characteristics of the generator and comparator junctions vary substantially from the ideal transition that defines a balanced comparator. In order to achieve the desired smooth transition of the switching characteristic we use biasing currents at $I_{\mathrm{b}} = 1.4$ and $1.5I_{\mathrm{c}}$. We now consider a range of different critical current spreads.

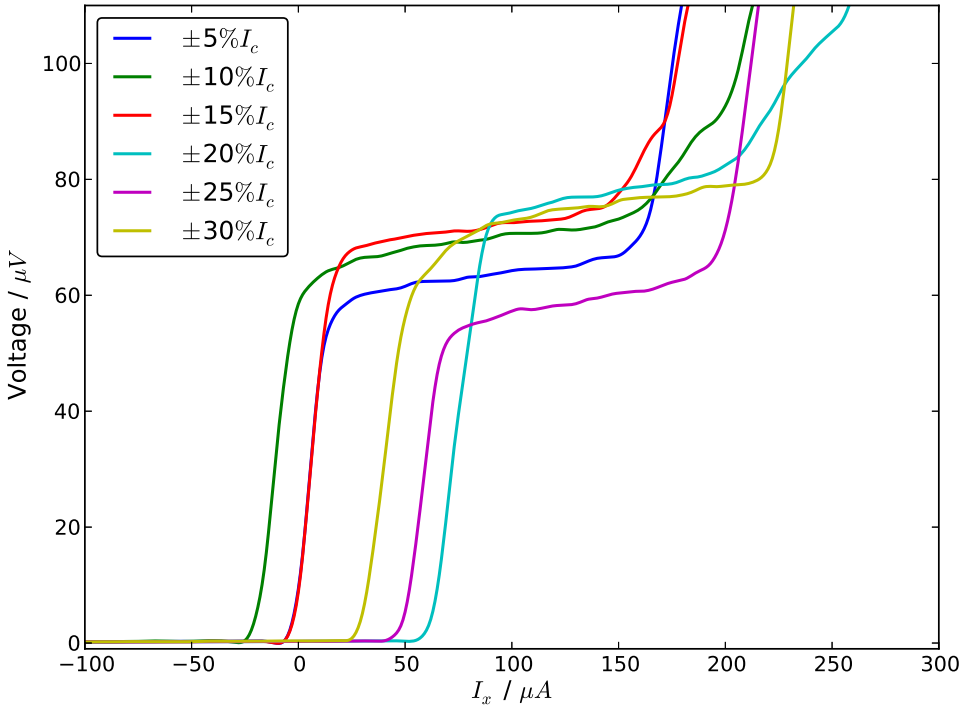
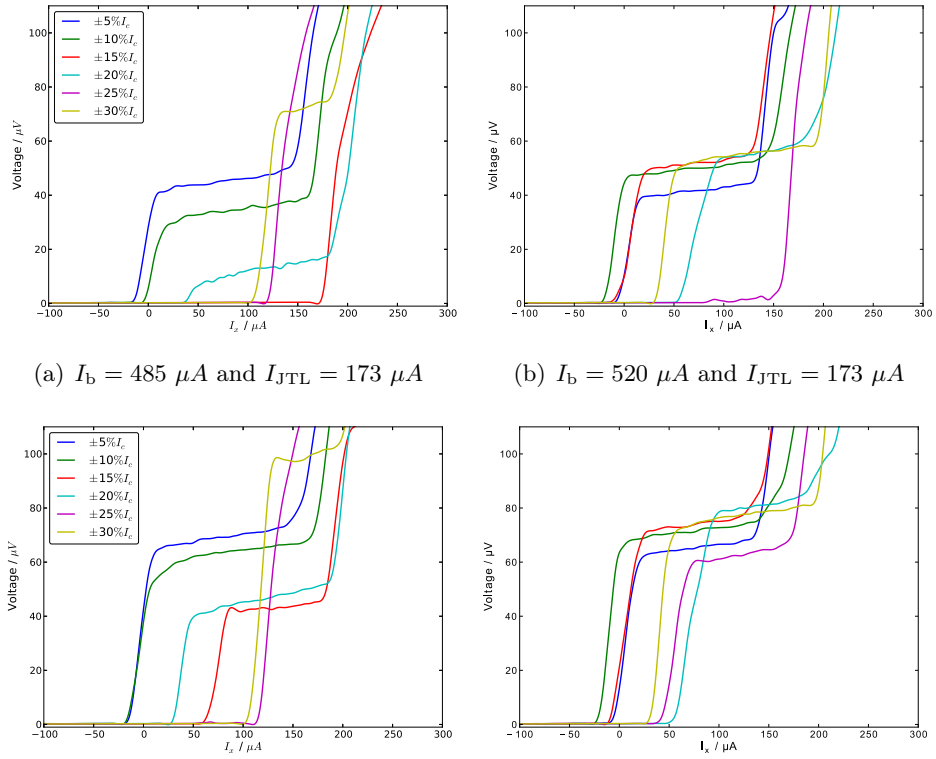


Figure 5.10: Switching characteristics of junction J_4 in the Josephson comparator at different critical current spreads. The observed shift in the threshold current I_{th} is seen in all the simulations and resembles the case of Oelze *et al.* seen in Chapter 4. This particular simulations is of a comparator with biasing values of $I_{\mathrm{g}} = 1.6I_{\mathrm{c}}$, $I_{\mathrm{b}} = 485\ \mu A$ and $I_{\mathrm{JTL}} = 0.6I_{\mathrm{c}}$. The further increase in voltage at higher I_{x} is where J_4 starts to self oscillate.

The addition of critical current spreads in Figure 5.10 results in a variation in the threshold current from $I_{\mathrm{th}} = 0\ \mu A$ when compared to the case where no spread is included. Expanding on this to other values of I_{b} and I_{JTL} as is shown in Figure 5.11 demonstrates possible operation of the Josephson comparator at

critical current spreads of up to and including ±30% of I_c and only requires re-biasing of the comparator to ensure correct function at all spreads for instance switching of junction J_4 at ±25% of I_c does not occur at $I_{JTL} = 0.5I_c$ as is shown in Figures 5.11(a) and 5.11(b). Increasing the value of I_{JTL} to $0.6I_c$ results in correct operation for all critical current spreads.



(a) $I_b = 485\ \mu A$ and $I_{JTL} = 173\ \mu A$

(b) $I_b = 520\ \mu A$ and $I_{JTL} = 173\ \mu A$

(c) $I_b = 485\ \mu A$ and $I_{JTL} = 208\ \mu A$

(d) $I_b = 520\ \mu A$ and $I_{JTL} = 208\ \mu A$

Figure 5.11: Simualted average voltage of junction J_4 of the Josephson comparator at $_c = 347\ \mu$A at $T = 8.4$ K with the addition of critical current spreads between $5 - 30\%$. The overall grey zone width (ΔI_x) recorded for $I_b = 520\ \mu$A and $I_{JTL} = 208\ \mu$A is 23, 17, 28, 24, 16 μA respectively, with each grey zone having a standard deviation of 6 μA. In comparison at $I_b = 485\ \mu$A and $I_{JTL} = 208\ \mu$A the recorded grey zone widths (ΔI_x stand at 16, 18, 23, 18 μA respectively with a standard deviation of 2 μA.

Grey zone width: We now consider the effect of variation in I_c on the resultant grey zone width, using the definitions of the grey zone described in Section 4.1. First we plot the resultant grey zone width ΔI_x GZ, GZ_1 and GZ_2

for simulations with critical current spread of $\pm 5\% I_c$ around the critical current calculated from the KO(I) theory for devices with a T_c of 9.25 K, a normal state resistant R_N of 1 Ω and temperatures, $T = 9,\ 8.5,\ 8,\ 7.5$ and 7 K. The results of this are reported in Figure 5.12.

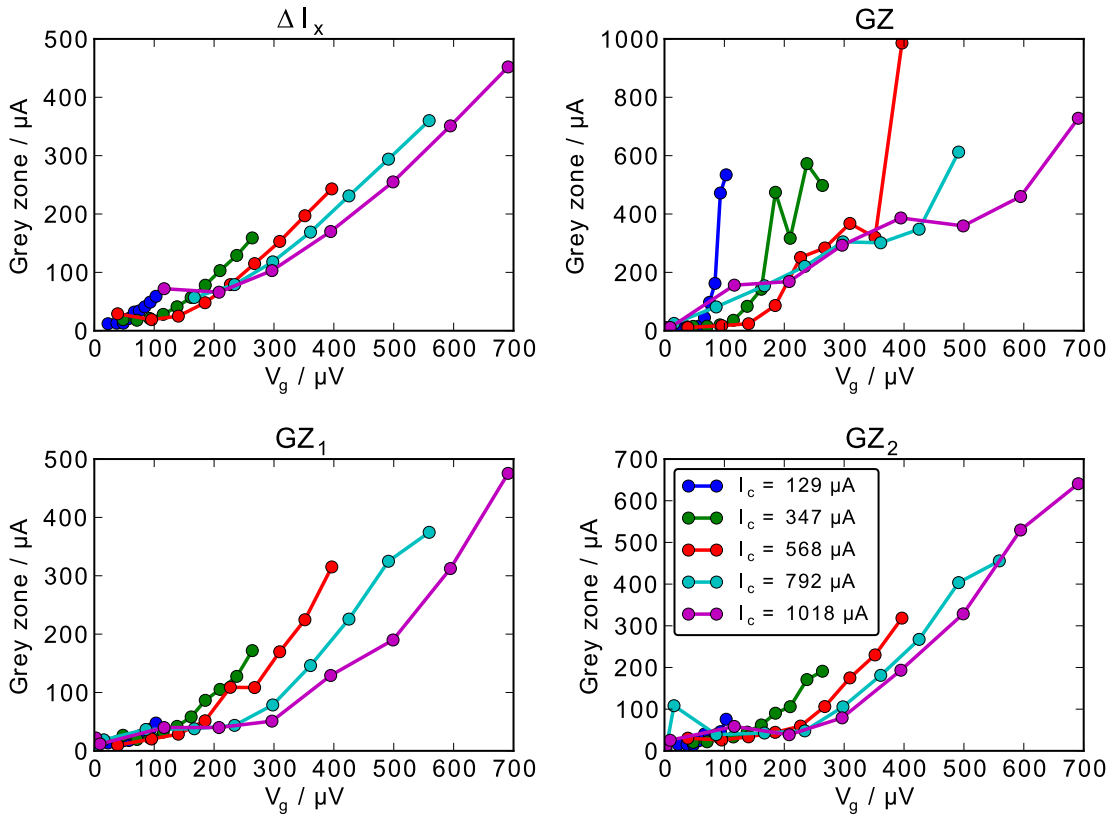


Figure 5.12: All the differently defined grey zones widths recorded for the Josephson comparator at critical current spread of $\pm 5\% I_c$ for $I_c = 347\ \mu A$, I_b at $1.4 I_c$ and I_g at $1.6 I_c$.

An increase in the value of I_c results in an increase of the possible range of voltage output achieved by J_g i.e. in the plot of ΔI_x the maximum grey zone width stands at 450 μA for an average voltage of 700 μV which translates into an operating frequency of 340 GHz. Whilst the large grey zone width makes operating at this point impractical it does speak towards the possibility of refinement resulting in the reduction of the grey zone at these kind of frequencies.

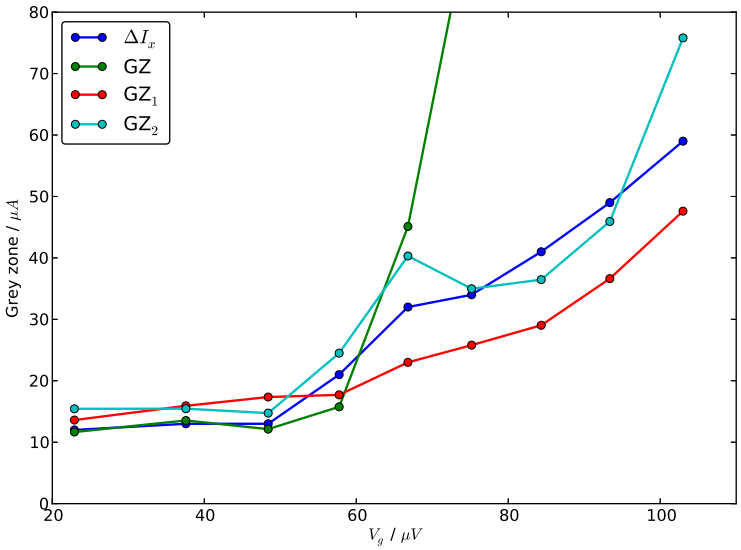


Figure 5.13: The recorded grey zone width dependence of the generator junction voltage for comparator device with $I_c = 129\ \mu A$.

Furthermore, examining the the grey zone width at lower operating voltage as is shown in Figure 5.13 for $I_c = 129\ \mu A$, we see that ΔI_x and GZ are in good agreement up to a value of $V_g = 50\ \mu V$ (which translates to an operating frequency of 24 GHz) with an almost constant grey zone width in this range similar to the recorded grey zone vs operating frequency observed by Haddad *et al.* [88] for a Nb tunnel junctions device (previously mentioned in Section 2.2.2 and in Figure 2.16).

The effect of critical current spreads on the grey zone width ΔI_x at $I_c = 129\ \mu$A is shown in Figure 5.14 demonstrates some discrepancies between the different critical current spreads at the lowest generator junction voltages. However the overall increasing trend of the grey zone is similar for all spreads and similarly, at the minima of the curves, the grey zone widths are similar. Expanding this to other critical currents as is shown in Figure 5.15 we see the effect of increasing I_c spread has on the recorded grey zone width.

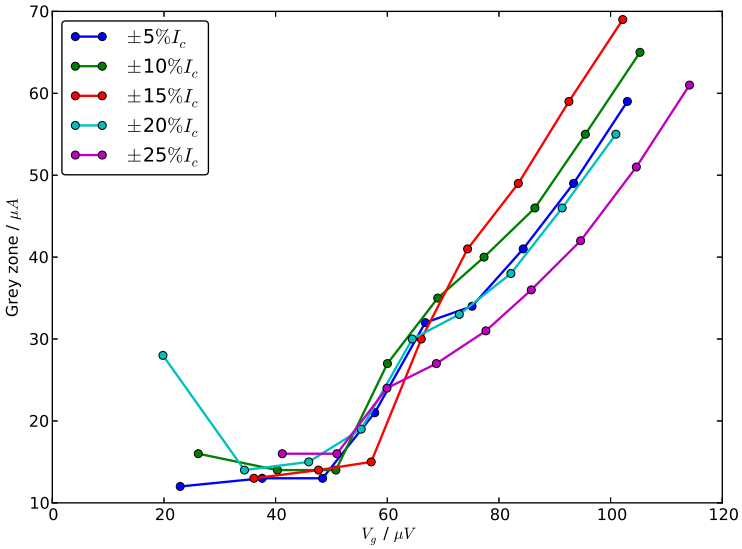
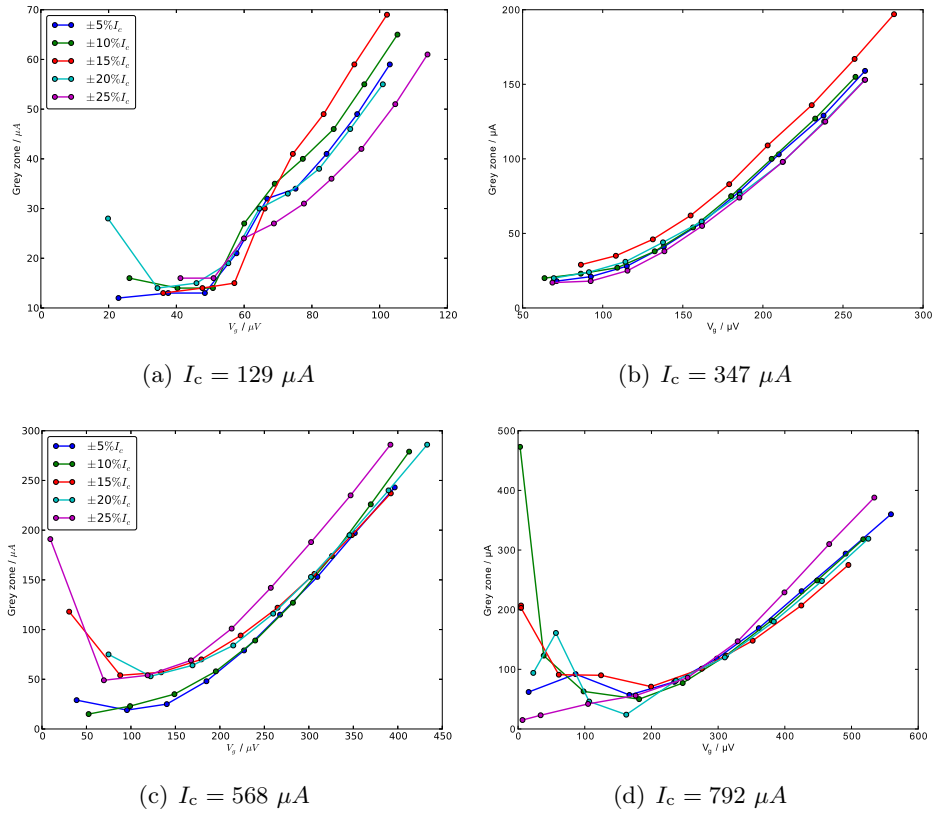


Figure 5.14: The recorded grey zone width dependence on the generator junction voltage for comparator device with $I_c = 129\ \mu A$ at different critical current spreads.

The Josephson comparator is still operational at higher critical current spreads but requires rebiasing of I_b in order to achieve minimum discrepancy between the different spread values, i.e. at bias of $I_b = 1.4I_b$ results in the least amount of fluctuations in the recorded grey zone width ΔI_x for $I_c = 129\ \mu A$ at all critical current spreads. At lower frequencies there is some fluctuations in the recorded grey zone for other critical currents. However this begins to settle as the frequency of the generator junction increases as is shown in Figure 5.15. The Josephson comparator has so far demonstrated quite a high tolerance rate for several values of critical current spreads reflecting variations in the length of the nanobridge weak link.

Whilst it would be ideal to maintain the lowest possible I_c spread for all active elements in the Josephson comparator, the use of the KO(I) theory and JSIM simulations suggests that comparators based on nanobridge weak link are quite resilient to variations in I_c and as such variations in the length of the nanobridge region of the weak link. In any case probably the variation in fabrication length will be less significant than the variation in width which we will examine next.



(a) $I_c = 129\ \mu A$ (b) $I_c = 347\ \mu A$

(c) $I_c = 568\ \mu A$ (d) $I_c = 792\ \mu A$

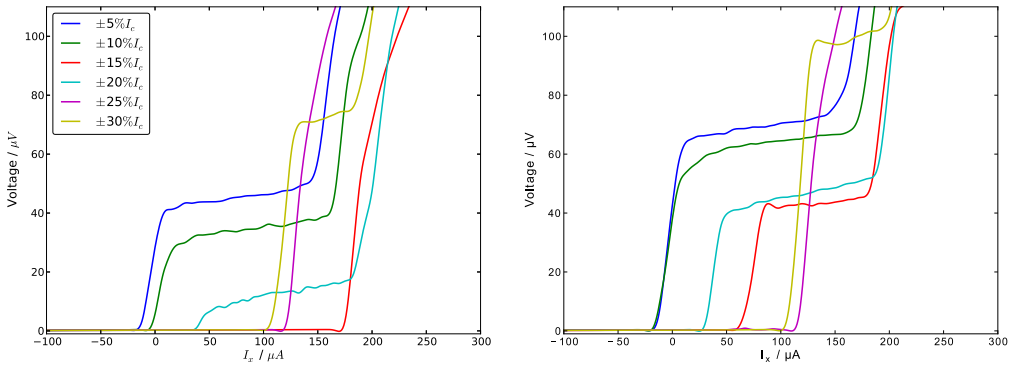
Figure 5.15: Recorded ΔI_x of the Josephson comparator at different critical currents and critical current spreads.

5.4 Variations of I_c and R_N with I_cR_N constant

In addition to variations in the length of the nanobridge weak link, using fabrication methods such as EBL or FIB will almost result in variation in nanobridge width. This will change I_c and R_N whilst keeping I_cR_N constant. To simulate this we fix I_cR_N using the KO(I) theory. We then allow I_c to vary and determine the corresponding R_N from I_cR_N.

Similar to what was established when I_c alone was varied, we begin by examining the result of corresponding variations in both I_c and R_N as shown in Figure 5.16 for junctions J_4 with a mean critical current of $I_c = 129\ \mu A$ and an I_cR_N product of 0.13 mV at $T = 9$ K. This shows possible operation of the Josephson comparator even at ±30% spreads in I_c and R_N with only some rebiasing of the device required

to achieve the desired switching characteristics.



(a) $I_\mathrm{b} = 485\ \mu A$ and $I_\mathrm{JTL} = 173\ \mu A$

(b) $I_\mathrm{b} = 485\ \mu A$ and $I_\mathrm{JTL} = 208\ \mu A$

Figure 5.16: Simulation of a Josephson comparator with variations in nanobridge width represented as a spread in I_c and R_N whilst maintaining the overall $I_\mathrm{c}R_\mathrm{N}$ to that of the KO(I) theory.

We estimate from SEM images of various arrays of nanobridges made at UCL and elsewhere that there could be spreads of ±10% in fabricated junction widths in even the best devices, so these simulated results are encouraging.

Grey zone width: The grey zone widths at the lowest spread of ±5% are shown in Figure 5.17. Like Figure 5.12, this demonstrates that the comparator performs very well at low critical currents, i.e. $I_\mathrm{c} = 129\ \mu A$, but access to higher values of operational frequencies requires an increase in I_c that comes at the cost of an increase in the resultant grey zone width.

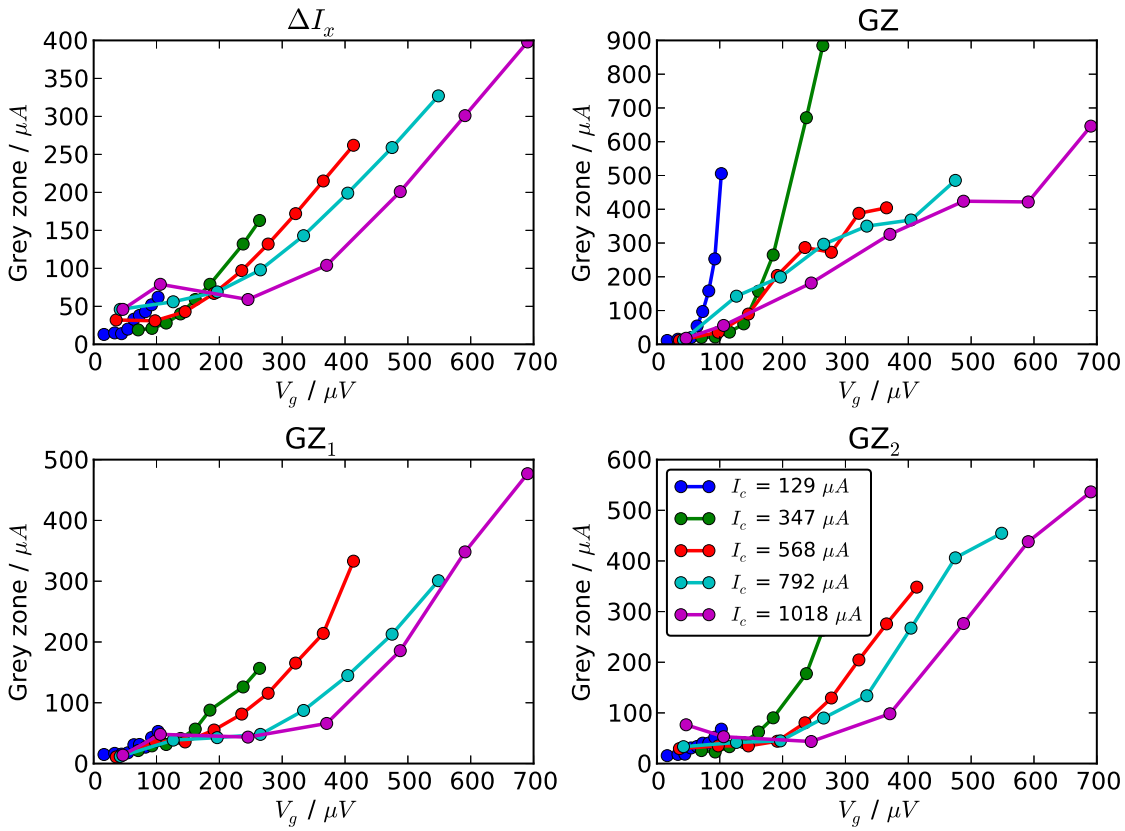
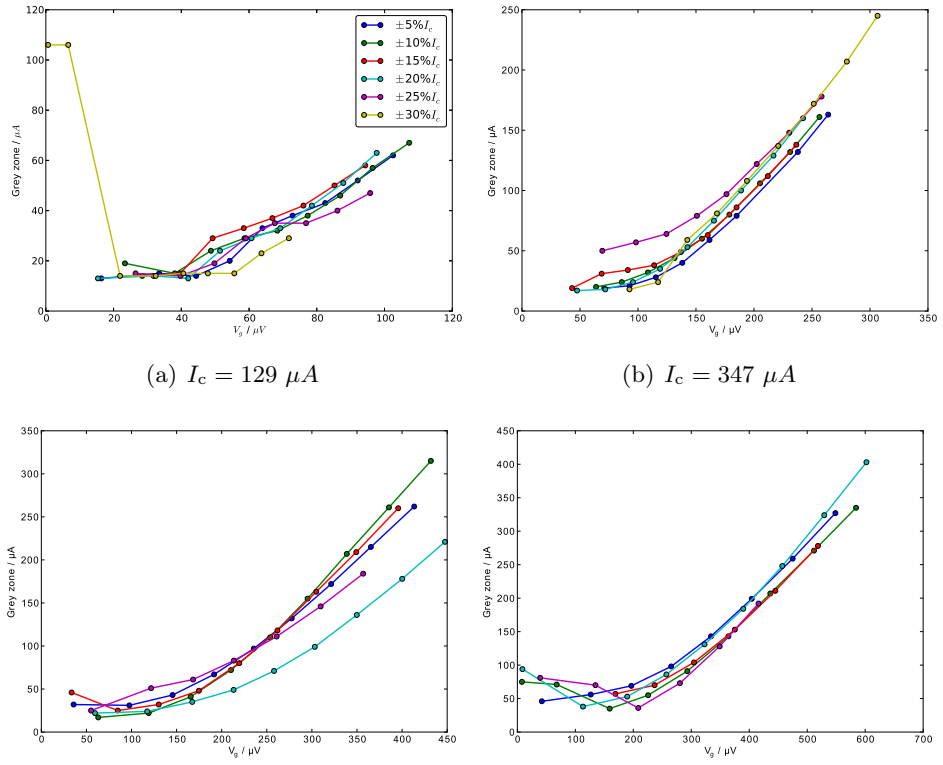


Figure 5.17: JSIM simulations of the grey zone width for a spread of ±5% in the critical current and the normal state resistance.

Expanding this to consider other spreads as shown in Figure 5.16 for different critical currents demonstrate similar characteristics to the simulations in Figure 5.15, i.e. an almost constant grey zone width at lower operational frequencies, as the frequency is increased the grey zone dependence on operational frequency increases linearly up to a maximum value at which point the device becomes inoperable.



(a) $I_c = 129\ \mu A$ (b) $I_c = 347\ \mu A$

(c) $I_c = 568\ \mu A$ (d) $I_c = 792\ \mu A$

Figure 5.18: Recorded ΔI_x of the Josephson comparator at different critical currents and critical current spreads with corresponding variations in R_N to keep $I_c R_N$ constant.

Similar to the case where only I_c was varied, we find the Josephson comparator based on nanobridge weak link parameters is very resistant to variation in the nanobridge width.

5.5 Summary

In this chapter we have outlined the effect of altering different parameters on the recorded grey zone width and the effectiveness of the device. By utilising the method introduced by Skocpol *et al.* [117] we were able to narrow down feasible operating temperatures to ensure that all Josephson comparators are operated in the non-hysteretic region. Variations in I_c and R_N can be used a simulation methods to represent variations in weak link length and width. applying spreads of up to $\pm$ 30% meant that results for the most common fabrication spreads can be investigated.

Due to the nature of the low T_c material and thus the corresponding operating temperatures, the device is very resistant to thermal noise fluctuations, instead a more pressing concern is the operating parameter β_L and the total loop inductance throughout the Josephson comparator. Performing simulations of with varied values of I_c we can replicate the effect of changes in the length of a weak link, whilst varying I_c and R_N, and adhering to the total I_cR_N product based on the KO(I) theory, we can simulate the effect of variations in both the length and the width of the weak link. In both scenarios the JSIM simulations demonstrate a functioning device that only requires rebiasing. In conclusion when all the results are considered this Josephson comparator is an ideal candidate as a low T_c device for RSFQ circuitry.

Chapter 6

Conclusions and suggested future work

6.1 Conclusion

In the present project, we have demonstrated simulations of Josephson junction superconducting circuitry using JSIM with a good degree of accuracy, the addition of noise whilst minimal at low temperatures makes JSIM a useful tool. Its use in conjunction with the KO(I) theory gives encouraging results as to the ability of nanobridge weak links to withstand successful variations in width and length due to fabrication methods. The simulations have also demonstrated the presence of an almost constant grey zone width at small critical current and operational frequency values. Operating at low critical current values results in a narrow grey zone although this however sacrifices the maximum operational frequency of the comparator.

The inductance of the JTL and comparator loops should be low enough so as to have a screening current $\beta_{\mathrm{L}} \approx 1$, leading both loops to hold only one flux quanta. An increase in the loop inductance results in the device occupying the storage state which in turn leads to the formation of a plateau indicative of the presence of extra flux in the system in turn reducing overall system sensitivity and

resulting in increased ΔI_x.

6.2 Future work

Whilst it is possible to operate the Josephson comparator at temperatures close to I_c, in an ideal scenario operation of the comparator would be well below T_c, as such the issue of hysteresis could be overcome through the use of a bilayer. By depositing a conductive layer such as gold on top of the Nb film, which has a better thermal conductivity and acts as thermal cap, with its higher thermal conductivity allowing heating to dissipate through it at a much faster rate than the formation of the hotspot.

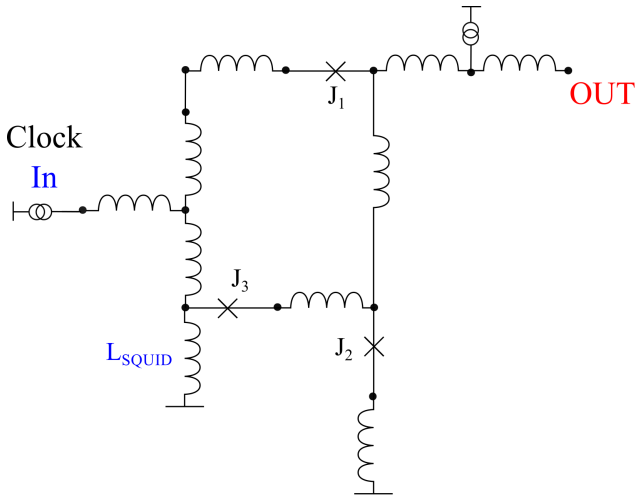


Figure 6.1: DC/SFQ circuit developed at SUNY/Stony Brook.

The versatility of the nanobridge weak links allows for the fabrication of several types of RSFQ circuits usually only obtained through cell libraries from specialised foundries such as HYPRES/Inc and SUNY/Stony Brook. One circuit of particular interest is the DC/SFQ converter in the SUNY/Stony Brook cell library shown in Figure 6.1. Built around a DC SQUID formed by $J_2 - L_{\mathrm{SQUID}} - (J_1/J_3)$ where junctions J_1 and J_3 act as a single junction. Once the signal current is large enough to trigger J_2 it causes in a flux to travel through to the output which could be a JTL whilst J_1 and J_2 ensure that the total flux in the loop remains at zero The net result "is that a single picosecond SFQ pulse can be generated on-chip by applying

a slowly changing, noisy and inexact dc current from a room-temperature current source. Similarly, when the input current is decreased below a certain value, the split junction J1,J3 flips, restoring the initial state of the SQUID". This would be a suitable circuit as a next step to try after nanobridge comparator.

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